MSC711xEVM User's Guide

StarCore DSP Evaluation Module

MSC711xEVMUG

Revision 0, April 2005

freescale™ semiconductor

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations not listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GMBH
Technical Information Center
Schatzbogen 7
81829 München, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Technical Information Center
3-20-1, Minami-Azabu. Minato-ku
Tokyo 106-8573, Japan
0120 191014 or +81-3-3440-3569
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T. Hong Kong
+800 2666 8080

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. StarCore is a trademark of StarCore LLC. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2004.

MSC711xEVMUG
Rev 0
4/2005

Contents

3 EVM Power and Connectors

4 EVM Functional Description

5 EVM Memory Maps and Bus Mapping

A MSC711xEVM Schematics

About This Book

This user's guide describes engineering specifications for the MSC711x evaluation module (EVM) board. This EVM board targets any of the StarLite MSC711x family of DSP processors. Each of these is a highly integrated system-on-a-chip device containing a StarCore™ SC1400 digital signal processing (DSP) cores.

The MSC711xEVM board is intended to serve as a platform for evaluating software developed for the StarLite processor environment. This manual lists and explains various features of the MSC711xEVM and describes how the board must be configured to test developed code for each processor.

Before Using This Manual—Important Note

The information in this manual is subject to change without notice, as described in the disclaimers on the title page of this manual. Before using this manual, determine whether it is the latest revision and whether there are errata or addenda. To locate any published errata or updates associated with this manual or this product, refer to the world-wide web site listed on the back cover of this manual or call your local distributor or sales representative.

Audience and Helpful Hints

This manual is for software developers and applications programmers who are developing products using the StarLite MSC711x device.

Notational Conventions and Definitions

This manual uses the following notational conventions:

mnemonics	Instruction mnemonics appear in lowercase bold.
italics	Book titles in text are set in italics. In addition, italics are used for emphasis and to highlight the main items in bulleted lists. Variables and equations are also italicized.
0x	Prefix to denote a hexadecimal number.
0b	Prefix to denote a binary number.

REG[FIELD]	Abbreviations or acronyms for registers appear in uppercase text. Following the register name, the bit or field name is enclosed in brackets. For example, ICR[8]:INIT refers to the Force Initialization bit (bit 8) in the host Interface Control Register.
Active high signals	Names of active high signals appear in small caps, sans serif, as follows: SIO1D[0–63], SIO1R, and GND_{PA}.
Active low signals	Signal names of active low signals appear in small capital letters in a sans serif typeface, with an overbar: $\overline{\text{SIOP1CS}}$, $\overline{\text{SIOP1WE[0–1]}}$, and $\overline{\text{SIOP1HT0}}$.
x	A lowercase italicized x in a register or signal name indicates that there are multiple registers or signals with this name. For example, SIOxA refers to the SIO0A and SIO1A signals. M*x*CBCR refers to the M0CBCR and M1CBCR registers.

Organization

Following is a summary and a brief description of the chapters of this manual:

- **Chapter 1**, *MSC711xEVM Overview*. Descriptive overview of main board specifications and MSC711xEVM features.
- **Chapter 2**, *Board Configuration and Installation*. Lists and explains necessary dipswitch and jumper configurations, test points and functional LEDs.
- **Chapter 3**, *EVM Power and Connectors*. Describes board power connector and supplies. Describes all board peripheral connectors.
- **Chapter 4**, *EVM Functional Description*. Describes the functionality of different segments of the board block diagram, such as I2C, EEPROM, and Fast Ethernet.
- **Chapter 5**, *EVM Memory Maps and Bus Mapping*. Describes the MSC711x memory map and the memory mapping for the HDI16 bus.
- ***Appendix A***, *MSC711xEVM Schematics.* Contains the schematics for the MSC711xEVM.

Related MSC711xEVM Documentation

- *MSC711x Reference Manual*
- *MSC7110 Technical Data Sheet*
- *MSC7112 Technical Data Sheet*
- *MSC7113 Technical Data Sheet*
- *MSC7116 Technical Data Sheet*
- *MSC7118 Technical Data Sheet*
- *MSC7119 Technical Data Sheet*
- *OCE10 On-Chip Emulator Reference Manual*
- *AKM AK4550 Codec Data Sheet.*
- *AKM AK4554 Codec Data Sheet.*
- *SWITI Switching Device PEF24471 HTSI-XL Wired Communication Data* sheet
- *VIA Technologies VT6103 Ethernet PHY Data Sheet.*

Abbreviations and Acronyms

List of abbreviations and acronyms:

ALU - Arithmetic Logic Unit

BCSR - Board Control and Status Register

COP - Common On-chip Processor

CPM - Communication Processor Module

CW - Metrowerks CodeWarrior IDE for StarCore

DIP - Dual-In-Line Package

DMA - Direct Memory Access

DSI - Direct Slave Interface

DSP - Digital Signal Processor

EOnCE - MSC711x on-chip emulation is now actualized by OCE10.

EVM - Evaluation Module

GPCM - Memory Controller General Purpose Chip-select Machine

GPL - General Purpose Line (associated with a UPM)

HCW - Hardware Configuration Word

HDI16 - Host Debug Interface 16 bit-wide

LSB - Least Significant Byte

lsb - least significant bit

Mbyte - Megabyte (1048576 bytes)

MII - Media Independent Interface

OCE10 - On-chip emulator. Provides a standard means of connecting a host computer running a debugger to a target system-on-chip.

PHY - Physical Layer

RMII - Reduced Media Independent Interface

SC711x - MSC711x family of devices.

SDRAM - Synchronous Dynamic Random Access Memory

SDRAM Machine - Memory Controller Synchronous Dynamic RAM Machine

SIU - System Interface Unit

SMII - Serial Media Independent Interface

SoC - System-on-chip.

TBD - To Be Defined

TDM - Time Division Multiplex

UART - Universal Asynchronous Receiver Transmitter

UPM - User Programmable Machine

UPM Machine - (Memory Controller) User Programmable Machine

ZD - Clock Zero Delay Buffer with internal PLL for skew elimination

MSC711xEVM Overview 1

This document is an operation guide for the MSC711x EVM board. It contains operational, functional and general information about the MSC711x evaluation module (EVM). This board is meant to serve as a platform for software and hardware development for the StarLite (MSC711x) family of processors. Each MSC711x chip is a highly integrated system-on-a-chip device containing a StarCore SC140 digital signal processor (DSP) core.

1.1 MSC711xEVM

This manual describes engineering specifications for the MSC711xEVM. Using its on-board resources and a debugger, a developer is able to download code, run it, set breakpoints, display memory and registers and connect proprietary hardware via the expansion connectors, to be incorporated into a desired system with the MSC711x processor.

The MSC711xEVM board is intended to serve as a platform for software development for the MSC711x processor environment. On-board resources and associated debugger enable developers to perform a variety of tasks:

- Download and run code,
- Set breakpoints,
- Display memory and registers,
- Connect proprietary hardware via the expansion connectors.

The MSC711x processor enables incorporation of these features into selected systems.

1.2 Board Specifications

Specifications for the MSC711xEVM board are provided in **Table 1-1**.

Table 1-1. MSC711xEVM Specifications

Characteristics	Specifications
Power requirements.	+5vdc @ 2A (Max.)
Microprocessor	MSC711x @ 100MHz bus, 200 MHz CPU

Table 1-1. MSC711xEVM Specifications (Continued)

Characteristics	Specifications
Memory DDR SDRAM (MSC711x)	32 Mbyte (32 bits wide)
Operating temperature.	$0^{o}C$ - $70^{o}C$
Relative humidity.	5% to 90% (non-condensing)
Dimensions:	100mm X 150mm

1.3 MSC711xEVM Features

The MSC711xEVM features are as follows:

- MSC711x as main DSP master.
- 32 Mbyte DDR SDRAM connected to the MSC711x - 32 bits wide.
- One 10/100 Base-T Ethernet port (MII) using VIA VT6103 connected to the MSC711x.
- One UART port connected to the MSC711x.
- 256Kbyte I^2C EEPROM connected to the MSC711x.
- OCE10/JTAG connector for the MSC711x.
- One UART port connected to the Host.
- HDI16 host available thru Header.
- COP/JTAG connector for the MPC711x.
- On-board parallel to JTAG Command Converter - connected to the MPC711x.
- Single +5V Power Supply.
- Power on indication LEDs for 5V, 3.3V, and 2.5V voltages.
- $\overline{\text{HRESET}}$ Push button for the MPC711x

Board Configuration and Installation 2

This chapter contains unpacking instructions, hardware preparation, configuration and installation information for the MSC711xEVM board. The user can check the configuration of the EVM board against the factory settings shown in this manual to ensure proper board functionality.

Caution: *Ensure that power is off or disconnected prior to reconfiguring an installed EVM board. Reconfiguring jumpers with the power on may damage system circuits.*

2.1 Hardware Unpacking

The first step in preparing the hardware is to unpack the EVM board. When unpacking the MSC711xEVM board from its shipping carton refer to the packing list to verify that all items are present and in good condition.

Note: If the shipping carton is damaged upon receipt, request carrier's agent to be present during unpacking and inspection of equipment. Unpack equipment from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing and reshipping of equipment.

2.2 Hardware Preparation

EVM board parameters can be changed for the following conditions:

- Force PC connection (Laptop or Desktop) - via JP1.
- Main Power Supply On/Off Switch - via SW4.
- MSC711x Power-up configuration - via SW3.
- Selecting Switch Inputs (software options) - via SW1.
- Ethernet PHY isolate -via JP3.

2.2.1 Board Configuration

Caution: *When configuring the board, avoid touching areas of integrated circuitry. Static discharge can damage circuits.*

To select the desired configuration and ensure proper operation of the MSC711xEVM board, changes of the configuration jumper and DIP switch settings may be required before installation. The location of the EVM's switches, indicators, DIP switches, configuration jumpers and connectors is shown in**Figure 2-1** .

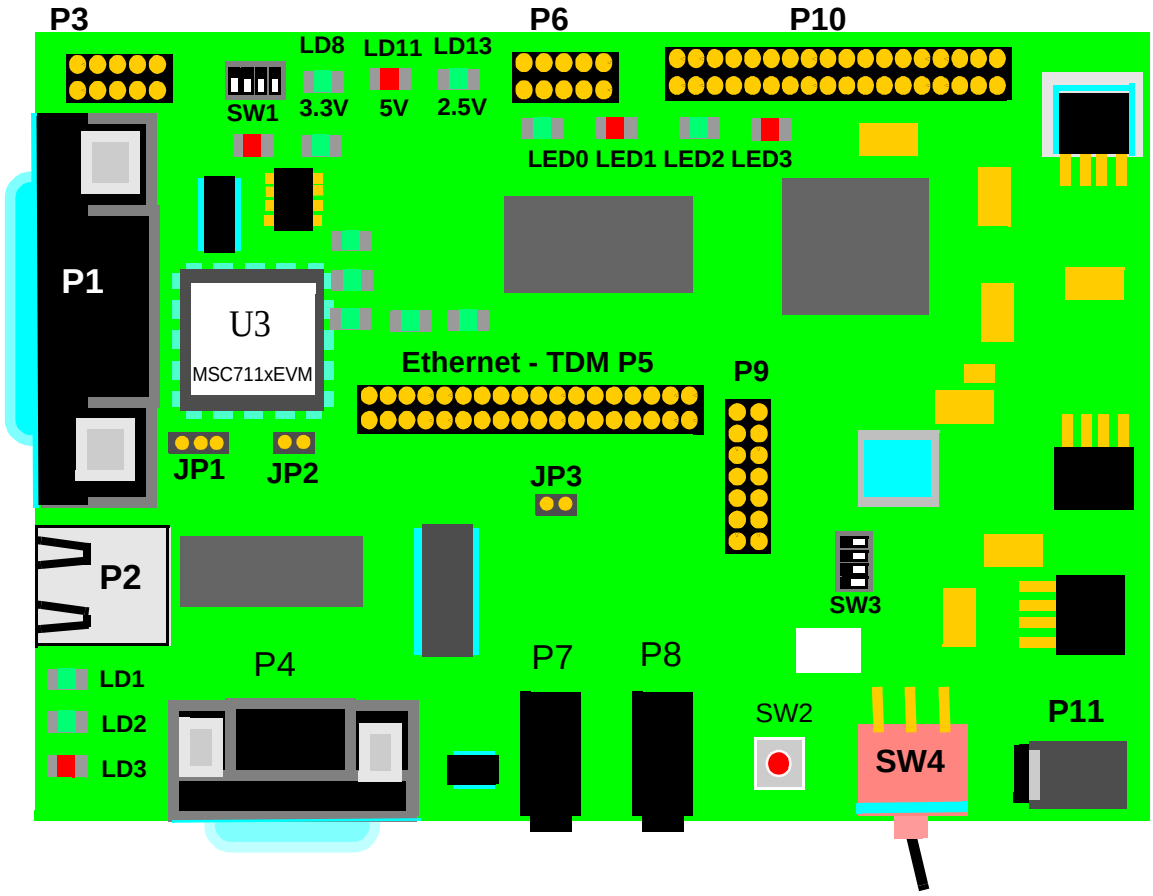


Figure 2-1. MSC711xEVM Top-side Part Location Diagram

The board has been factory tested and is shipped with DIP switch settings as described in the following paragraphs.

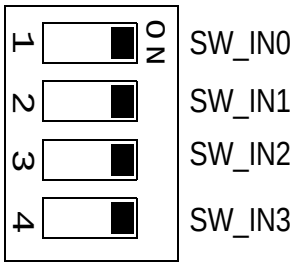
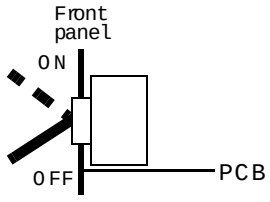
2.2.2 I²C EEPROM Configuration

The I²C EEPROM Configuration Bus ADDRESS is "000" - determined by pull down resistors. The Write Protection Mode for the EEPROM is disabled at the factory. However, "OPTION" pull up resistors are available on the EVM to change the default settings. You can enable Write Protection, and change the EEPROM address.

2.2.3 Switches and DIP Switches

EVM pushbuttons, switches and DIP subswitches are listed and described in **Table 2-1**. Switch locations are shown in **Figure 2-1**. The switches discussed in the table are shown with their factory default positions.

Table 2-1. EVM Switches

Designator and Purpose	Type	Description
User Configurable DIP Switch SW1 **Starlite GPIO Inputs**	 GPIO Inputs	Subwitches **SW1-1 thru SW1-4** are inputs in the MSC711x. They are user configured by software as one of three signals at the pin. SW1.1 - StarLite pin Y13 (T1RCK/IRQ0/GPIO). SW1.2 - StarLite pin V13 (T1RFS/IRQ1/GPIO). SW1.3 - StarLite pin W13 (T1RD/IRQ8/GPIO). SW1.4 - StarLite pin V13 (T1TCK/IRQ9/GPIO). If the subswitch is in the “ON position, its related signal is at “0”. If the subswitch is in the “OFF” position, related signal is at “1”. **Factory settings:** All subswitches “ON”, signal at “0”.
Pushbutton SW2 **MSC711x Hard Reset**		Press pushbutton SW2 for an MSC711x hard reset. The HRESET signal is de-bounced.
Power-up Configuration DIP Switch SW3	 Power-up Settings	Subswitch **SW3.1** is the Debug Request. When the subswitch is “ON”, the MSC711x is in Debug mode. Subswitch **SW3.2** disables the Software Watchdog Timer. This pin is sampled on the negation of PORESET. Subswitch **SW3.3** and **SW3.4** define the Boot Mode of the MSC711x. Pins are sampled on the negation of PORESET. If the subswitch is in the “ON position, its related signal is at “0”. If the subswitch is in the “OFF” position, related signal is at “1”. **Factory settings:** All subswitches “ON”, signal at “0”.
SW4 **Main Power Switch**		When the switch is “ON”, the EVM is powered from an external 12V power supply via the PX connector. When the switch is “OFF” the external power supply is disconnected. Toggling the switch turns the main power on and off.

2.2.4 EVM Configuration Jumpers

The MSC711xEVM configuration jumpers and their settings are explained in the following sub-sections. Jumper locations are shown in **Figure 2-1**, *MSC711xEVM Top-side Part Location Diagram*, on page 2-2. The jumpers are shown with their factory default positions.

2.2.4.1 JP1-Host Terminal Connection

JP1 selects whether the host terminal connection to the MSC711xEVM is to be made for a Laptop or for a Desktop PC. Jumpering pins 1 and 2 forces a laptop connection to the EVM while a jumper on pins 2 and 3, or no jumper on JP1 at all, forces a desktop connection. The factory setting is pins 2 and 3 jumpered. The relative states of JP1 pins are illustrated below in
.

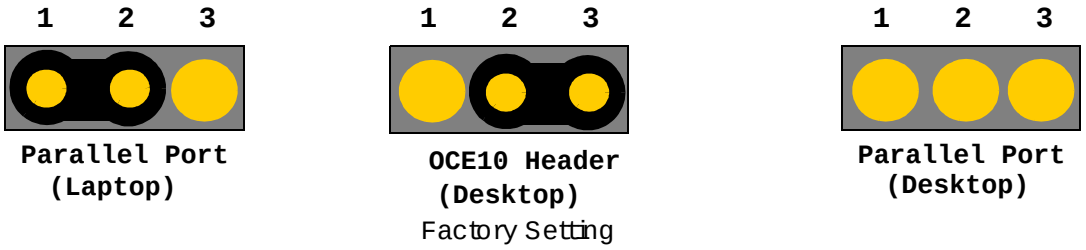


Figure 2-2. JP1- Host Terminal Connection

When a jumper is present on pins 1 and 2 of JP1, this means there is a GND in JP1. This is a special mode for working with a laptop. When no jumper is present in JP1, or pins 2 and 3 are jumpered, the EVM is in Desktop mode (Default).

2.2.4.2 JP2-Not Used

The prototype boards still contain configuration jumper header JP2. This jumper will be removed in later versions and its setting has no effect on board operation.

Figure 2-3. JP2 - Not Used

2.2.4.3 JP3-Ethernet PHY Mode

Jumper JP3 to measure or set the MSC711x EE0 signal logic levels. If you wish to close JP3, place a jumper on pins 1 and 2, as shown below. The factory setting is “Open”.

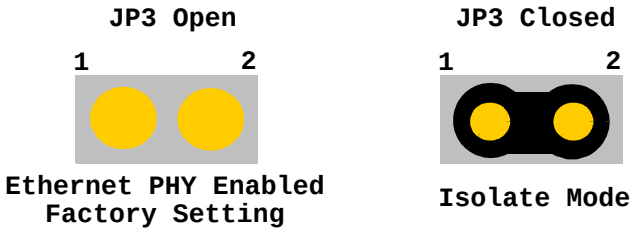


Figure 2-4. JP3-Ethernet PHY Mode

2.2.5 EVM Testing

MSC711xEVM testing is detailed in the following sub-sections. The location of the various EVM test points and bridges is shown in **Figure 2-1**, *MSC711xEVM Top-side Part Location Diagram*, on page 2-2.

2.2.5.1 TP1 - TP20 Signal Measurment

TP1- TP20 allow testing for the I^2C signals and the CPLD as shown in **Table 2-2**.

Table 2-2. Signal and CPLD Test Points

TestPoint	Connection
TP1 - TP13	Connected to the CPLD for R&D use only.
TP14	I2CSD - I^2C Serial Data
TP15	I2CSCL - I^2C Clock
TP16 - TP20	Connected to the CPLD for R&D use only.

2.2.5.2 TP21-TP27 Voltage Measurement

EVM voltage test points reside, respectively, on the voltages shown in **Table 2-3**.

Table 2-3. Voltage Test Points

Test Point	Sampling	Test Point	Sampling
TP21	DDR VTT	TP25	2.5V
TP22	DDR Vref	TP26	5V
TP24	3.3V	TP27	1.2V

2.2.5.3 JS1-JS3 GND Bridges

The MSC711xEVM has three bridges designated as GND. The bridges assist in general measurements and act as logic analyzer connections.

Caution: *Only use INSULATED GND clips when connecting to a GND bridge. Otherwise, permanent damage may occur to the MSC711xEVM. Non-insulated clips that come into contact with surrounding "HOT" points may cause short-circuits.*

2.2.6 EVM LEDs

The MSC711xEVM operational LEDs are described in the following sub-sections. The LED locations are shown in **Figure 2-1**, *MSC711xEVM Top-side Part Location Diagram,* on page 2-2.

Table 2-4. ADS LEDs Functions

LED	Function
LD1 MSC711x Fast Ethernet Port Link Indicator	Green LD1 lights when there is a physical link connection in the RJ45 connector P2.
LD2 MSC711x Fast Ethernet Port 100Base-Tx Indicator	Green LD2 lights when the VT6103 on the MSC711x is enabled and is in 100 Mbps operation mode.
LD3 MSC711x Fast Ethernet Port Full Duplex Indicator	Red LD3 lights when the VT6103 on the MSC711x is enabled and is in Full Duplex operation mode.
LD4 I^2C EEPROM CLOCK:SCL	Red LD4 is connected to the Clock Line of the I^2C BUS.
LD7 External Debugger Connection Indicator	When lit, green external debugger connection LD7 indicates that the parallel port cable is not attached to the EVM board. The user can connect to the board using third company external device via OCE10/JTAG connector P9. When the parallel cable is connected at P1, LD7 turns off and communication is made by an internal device.
LD8 3.3V Indicator	Green LD8, indicates the presence of the +3.3V supply on the board.
LD9 I^2C EEPROM DATA:SDA	Green LD9 is connected to the Data line of the I^2C Bus.
LD11 5V Indicator	Green LD11, indicates the presence of the +5V supply on the board.
LD13 2.5V Indicator	Green LD13, indicates the presence of the +2.5V supply on the board.
LD14 General Purpose LED 0 Indicator	General purpose red LD14 is user controlled by GPIO pin W14.
LD15 General Purpose LED 1 Indicator	General purpose red LD15 is user controlled by GPIO pin V14.

Table 2-4. ADS LEDs Functions (Continued)

LED	Function
LD16 **General Purpose LED 2 Indicator**	General purpose red LD16 is user controlled by GPIO pin W12.
LD17 **General Purpose LED 3 Indicator**	General purpose red LD17 is user controlled by GPIO pin W14.

EVM Power and Connectors 3

The location of the MSC711xEVM power, communication and expansion connectors is shown in **Figure 3-1**.

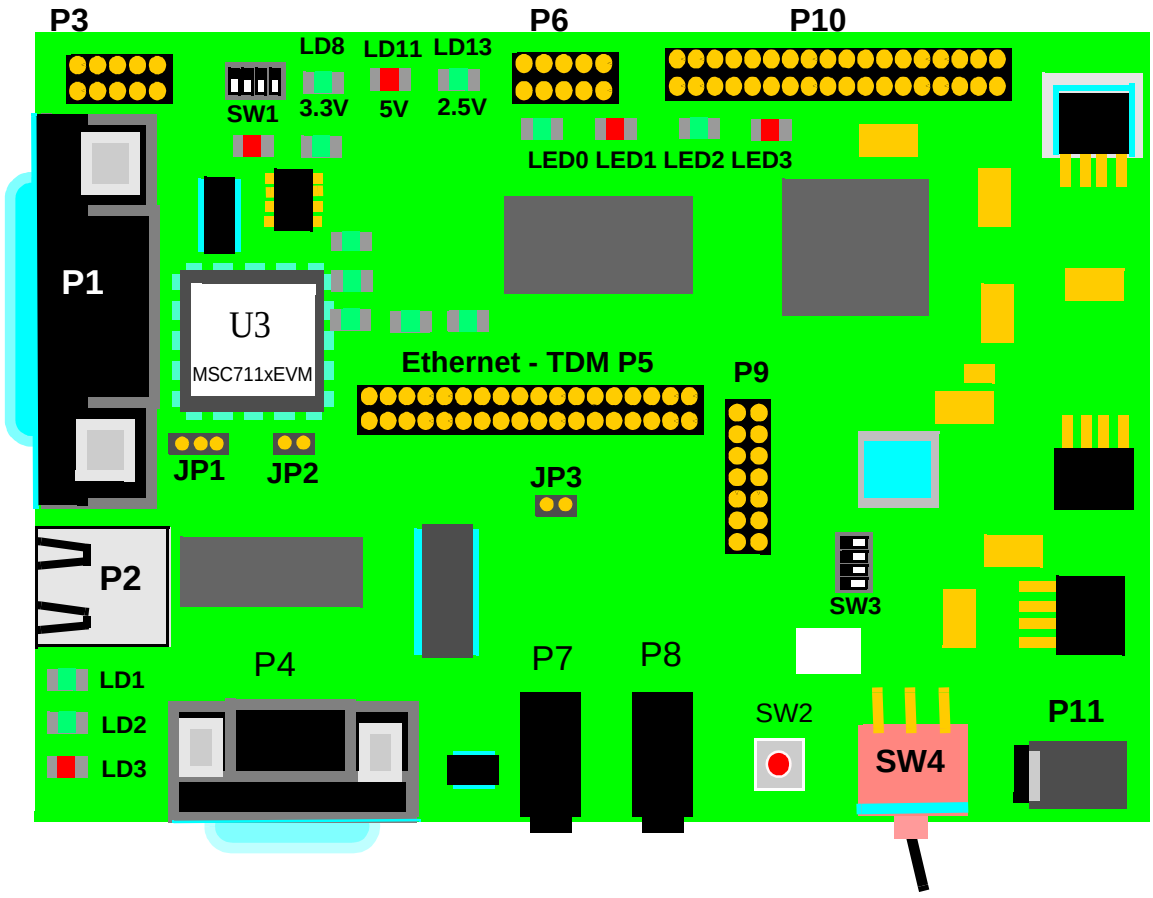


Figure 3-1. MSC711xEVM Connector Locations

3.1 Power

Power is supplied to the MSC711xEVM via EVM connector P11. P11 is a 2mm Power Jack RAPC722 providing connection to an external +5VDC @ 2A power supply.

3.1.1 Required MSC711xEVM Voltages

For normal operation, the MSC711xEVM requires the following voltages:

- 5V : (Main Power supply).
- 3.3V : (MSC711x I/O and for most of the components).
- 2.5V : (SSTL components: the DDR chip and the DDR interface in the MSC711x).
- VTT : (1.25V for DDR active termination).
- 1.2V : MSC711x core voltage.

The MSC711x chip evaluation maximum current demands are:

- 100mA for the I/O @ 3.3V.
- 240mA for the SSTL_IO +DDR @ 2.5V.
- 511mA for the core @ 1.2V.

3.1.2 Power Supply

The MSC711xEVM requires a power supply of +5V DC @ 2A max. To apply power directly to the EVM board, insert enclosed power supply plug into the board's P11 power jack.

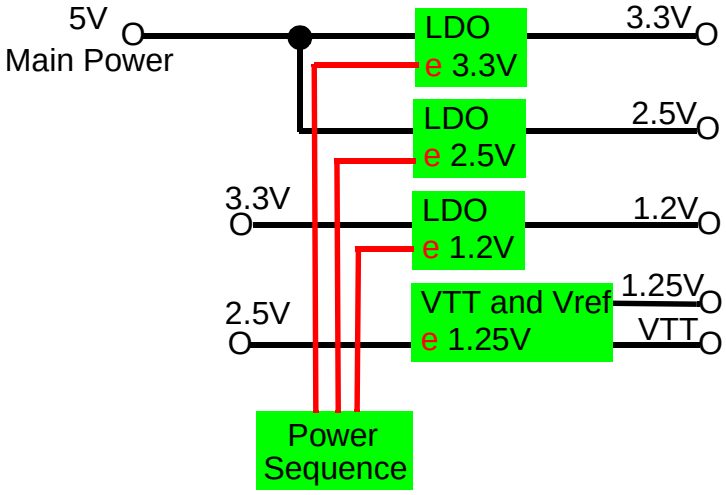


Figure 3-2. Power Supply Block Diagram.

The power supply is made up of five separate unrelated devices:

- The main 3.3V voltage produced from a LDO NATIONAL_LP3872_3V3, This module is capable of delivering 1.5A max current.
- The 2.5V is produced by an LDO device NATIONAL_LP3872_2V5 capable of handling 1.5A.

- The 1.2V is produced by a LDO device MIC29302BU from Micrel capable of handling 1.5A.
- The VTT / VREF is produced by a LDO device FAN1655MTF from Fairchild capable of handling 2.1A.

3.1.3 Power Sequence

The MSC711xEVM has 3 distinct power supplies: 1.2V core, 2.5V DDR I/O, 3.3V Standard I/O. It is extremely important to observe strict power-up sequence at the board level to avoid latch up forward biasing of ESD devices and excessive currents.

Caution: *Improper power-up sequencing can lead to severe device damage.*

From a time variant viewpoint, during power ramping up, at any instant, the 2.5V supply must maintain a differential of +0.7V or more below the 3.3V supply. Also, at any instant, the 1.2V supply must maintain a differential of +0.7V or more below the 2.5V supply. This restriction includes the power-up sequence.

3.1.3.1 Power-Up Sequence

The following must be the sequence for power-up:

1. Turn on highest supply first. (3.3V Standard I/O).
2. Turn on 2.5V DDR I/O supply.
3. Turn on last lowest supply 1.2V core.

3.1.3.2 Power Sequence Control Logic

The MSC711xEVM power sequence control logic circuit is a 3.3V monitor and an internal counter realized in the Altera CPLD device. These provide the necessary delays in power up sequence.

3.1.4 EVM Power Connection Procedure

Since the power sequencing is automatically provided by the CPLD device, to power-up the board, the user need only plug the external power into board connector P11, then toggle the power switch SW4. This powers the board up in the correct power up sequence.

3.2 EVM Interconnect Signals

The MSC711xEVM interconnects with external devices via the following connectors:

- P1 - 25 Pin D type female port, main communication port between the computer and the MSC711x in SPP mode.
- P2- RJ-45 100/10 Base-T Ethernet port
- P3 - In System Programming (ISP) for configuration of the CPLD
- P4 - D-type 9 Pin 90^0 female RS-232 port
- P5 - 36 Pin male header , connects to TDM and Ethernet signals.
- P6 - 10 Pin male header, connects to Power On configuration signals.
- P7 - Stereo Line In Phone Jack.
- P8 - Stereo Line OutPhone Jack.
- P9 - JTAG/OCE10
- P10 - HDI header

3.2.1 Main Communication Port (P1)

EVM connector P1 is main communication port with the MSC711x. It is a 25 Pin female Dtype connector. Connector P1 signals are described in **Table 3-1**.

Table 3-1. Connector P1 Signals

Pin Number	EPP Function	SPP Function
1	Write	
2	DB0	RESET
3	DB1	TMS_IN
4	DB2	TCK_IN
5	DB3	TDI_IN
6	DB4	TRST_IN
7	DB5	DR_IN
8	DB6	IDENT
9	DB7	
10	IRQ	
11	Wait	TD0_OUT
12 and 15	N.C.	
13	Select	5V_OUT
14	Dstrobe	
16	Reset	
17	Astrobe	
18 - 24	GND	
25	IN	

3.2.2 RJ45 Ethernet Line Connector (P2)

The Ethernet line connector (P2), a twisted-pair compatible connector, is implemented with a 90^{o}, 8-pin, RJ45 connector. Connector P2 signals are described in **Table 3-2**.

Table 3-2. P2: Ethernet Port Interconnect Signals

Pin No.	Signal Name	Description
1	TPTX(GRAY)	Twisted-Pair Transmit Data positive **output** from the MSC711xEVM.
2	TPTX~(BROWN)	Twisted-Pair Transmit Data negative **output** from the MSC711xEVM.
3	TPRX(YELLOW)	Twisted-Pair Receive Data positive **input** to the MSC711xEVM.
4, 5	(RED,GREEN)	Bob Smith terminated on the MSC711xEVM.
6	TPRX~(BLACK)	Twisted-Pair Receive Data negative **input** to the MSC711xEVM.
7, 8	(BLUE,ORANGE)	Bob Smith terminated on the MSC711xEVM.

3.2.3 In System Programming (ISP) Connector (P3)

Connector P3 is a 10-pin generic 0.050" pitch header connector providing in-system programming capability for the board CPLD device (for board programmable logic). P3 pinout is seen in **Table 3-3**.

Table 3-3. ISP Connector-Interconnect Signals

Pin No.	Signal Name	Attribute	Description
1	TCK	I	ISP test port clock. This clock shifts in/out data to/from the programmable logic JTAG chain.
2	GND	P	Digital GND. Main GND plane.
3	TDO	O	ISP Transmit Data Output. Programmable logic of the JTAG serial data output driven by falling edge of TCK.????
4	VCC	P	Connect to 3.3V power supply bus for feeding an external programmer logic.
5	TMS	I	ISP Test Mode Select. This signal is qualified with TCK - changes the state of the programmable logic JTAG machine.
6	N.C.	-	Not Connected.
7	N.C.	-	Not Connected.
8	N.C.	-	Not Connected.
9	TDI	I	ISP Transmit Data In. Programmable logic of the JTAG serial data input.
10	GND	P	Digital GND. Main GND plane.

3.2.4 Slave UART Port Connector (P4)

Port P4 is connected to the UART port on the MSC711x Device. This is implemented by an ICL3221 transceiver, which internally generates the required RS-232 levels using a single 3.3V supply. The transceiver is always enabled.

The slave UART RS-232 port connector (P4) is a 9-pin, 90°, female D-type shielded connector. The RS-232 pins can be switched to drive an expansion connector.

RS-232 ports' pins are shown in **Figure 3-3**. In this figure, TX (Output) is “Transmit Data” and RX (Input) is “Receive Data”..

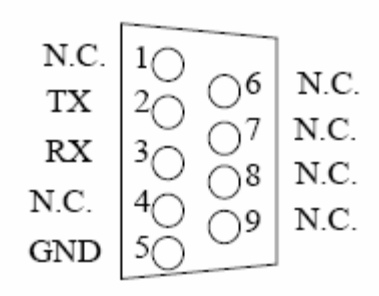


Figure 3-3. MSC711x RS-232 Serial Ports' Connector

P4 signals are outlined in **Table 3-4**.

Table 3-4. UART RS-232 Interconnect Signals

Pin No.	Signal Name	Description
1, 4, 6, 7 8, 9	N.C.	These pins are not connected in this port.
2	TX	Transmit Data **output** from the MSC711xEVM.
3	RX	Receive Data **input** to the MSC711xEVM.
5	GND	Ground signal of the MSC711xEVM.

3.2.5 SMD Header P5

The SMD header, P5, is a 36 pin connection to both the TDM and the Ethernet signals. The pin out is shown in **Figure 3-4**.

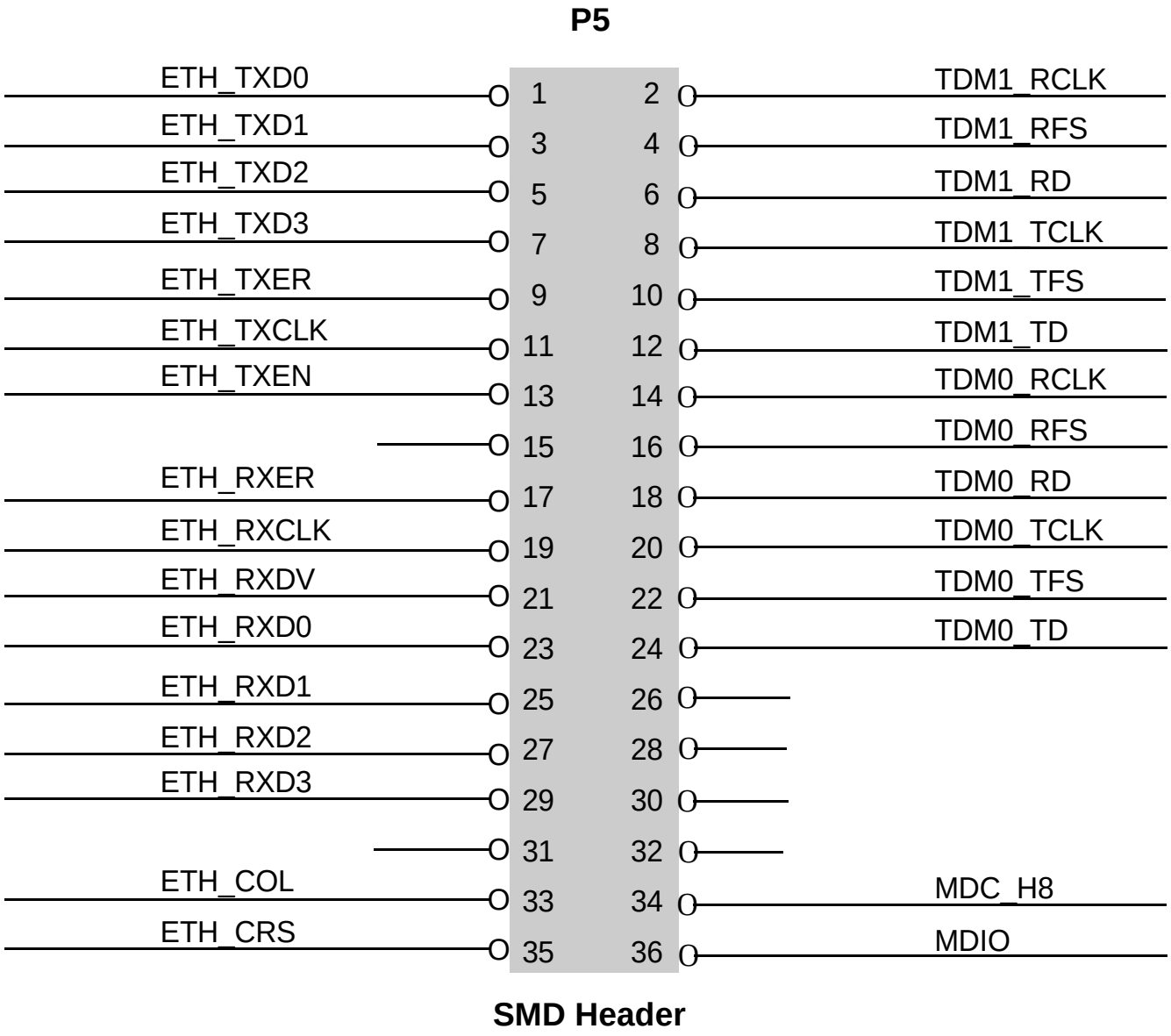


Figure 3-4. SMD Header Signals

Table 3-5. HDI Header Signals

Pin No.	Signal Name	Attribute	Description
1	GND	p	Digital GND. Main ground plane.
2			
3	HD0	I/O	Host Interface Bidirectional, three-stated Data Bus Port: HD (0 - 15)
4	HD1		
5	HD2		
6	HD3		
7	HD4		
8	HD5		
9	HD6		
10	HD7		
11	HD8		
12	HD9		
13	HD10		
14	HD11		
15	HD12		
16	HD13		
17	HD14		
18	HD15		
19	GND	P	Digital GND. Main ground plane.
20			
21	HA0	I	Host Interface Address Line HA (0 : 3)
22	HA1		
23	HA2		
24	HA3		
25	HCS1	I	Host Chip Select 1. The HDI CS is determined by the logical OR between HCS1 and HCS2.
26	HCS2	I	Host Chip Select 2. The HDI CS is determined by the logical OR between HCS1 and HCS2.
27	HACK	I/O, T.S.	Host Acknowledge or Receive Host Request Output. **Host DMA Acknowledge/Host Receive Request** When the HDI16 is programmed to interface to a single host request, this pin is the host acknowledge Schmitt trigger input in host DMA mode (HACK). The polarity of the host DMA acknowledge is programmable.

3.2.6 Power-On Configuration Header (P6)

The signals received on the 10 Pin male header P6 are explained in **Figure 3-5**.

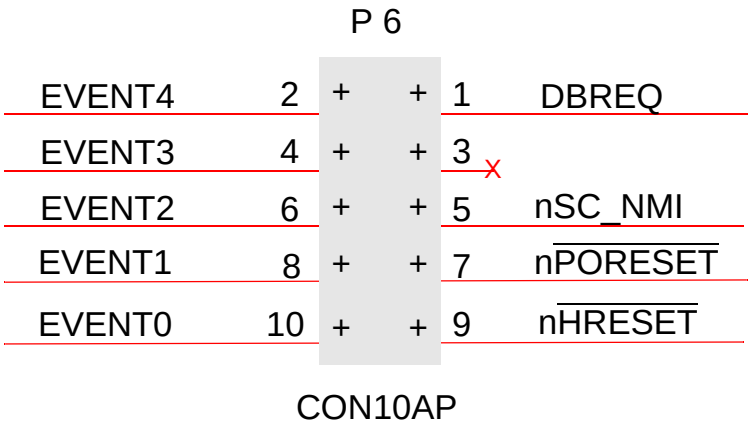


Figure 3-5. Header P6 - Power-On Configuration Signals

3.2.7 Stereo Phone Jack Connectors (P7, P8)

EVM connector P7 is the stereo line in phone jack, while connector P8 is the stereo line out phone jack.

3.2.8 Host Debug OCE10 (SYS) Connector (P9)

Connector P9 is a Freescale standard DSP JTAG/OCE10 connector featuring a 14-pin, 90^{o} 2-row header connector with key. Host debug accesses all processors joined by the JTAG chain via connector P9. This connector's pinout shown in **Table 3-6**.

Caution: *When driven by an external tool, pin 9 ($\overline{HRESET}$) MUST be driven with an Open Drain gate. Failure to do so may result in permanent damage to the MSC711xEVM logic.*

Table 3-6. JTAG/OCE10 Connector-Interconnect Signals

Pin No.	Signal Name	Attribute	Description
1	TDIh	I	Transmit Data In. MSC711x's JTAG serial data input - sampled on the rising edge of TCK.
2	GND	P	Digital GND. Main GND plane.
3	TDOhc	O	Transmit Data Output. DSP JTAG serial data output driven by falling edge of TCK.
4	GND	P	Digital GND. Main GND plane.
5	TCKhc	I	Test port clock. The clock shifts in/out data to/from JTAG logic. Data is driven on the falling edge of TCK and sampled both internally and externally on it's rising edge.
6	GND	P	Digital GND. Main GND plane.
7	N.C.	-	Not Connected.
8	KEY	-	No pin in connector. Serves for correct plug insertion.
9	$\overline{HRESET}$	I/O,P.U.	When asserted by external H/W Hard-Reset sequence is generated. During that sequence the MSC8103 asserts for 512 system clocks. Pulled-up on the ADS using a 1KW resistor. **When driven by an external tool it MUST be driven with an Open Drain gate. Failure to do so may result in permanent damage to the MSC711x and/or to EVM logic.**
10	TMSh	I	Test Mode Select. Signal is qualified with TCK in a same manner as TDI - changes the state of the JTAG machines. The line is internally pulled-up by the MSC8103.
11	VDD	P	Connect to 3.3V power supply bus via protection resistor. May be used for Command Convertor power.
12	N.C.	-	Not Connected.
13			
14	$\overline{TRST}$hb	I	Test port reset. When signal is active (low) it resets the JTAG logic. The line is pulled-down on the ADS with a 2.2KW resistor in order to provide continuous JTAG logic reset when the connector is unplugged.

A front view of Connector P9 is shown in **Figure 3-6**.

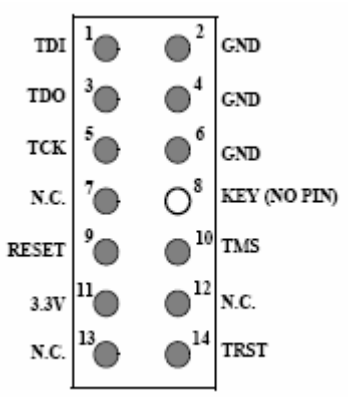


Figure 3-6. JTAG/OCE10 Connector, Front View

3.2.9 Host Interface (HDI) Connector (P10)

Signals related to the individual pins of header P10, the HDI connector, are shown in **Figure 3-7**.

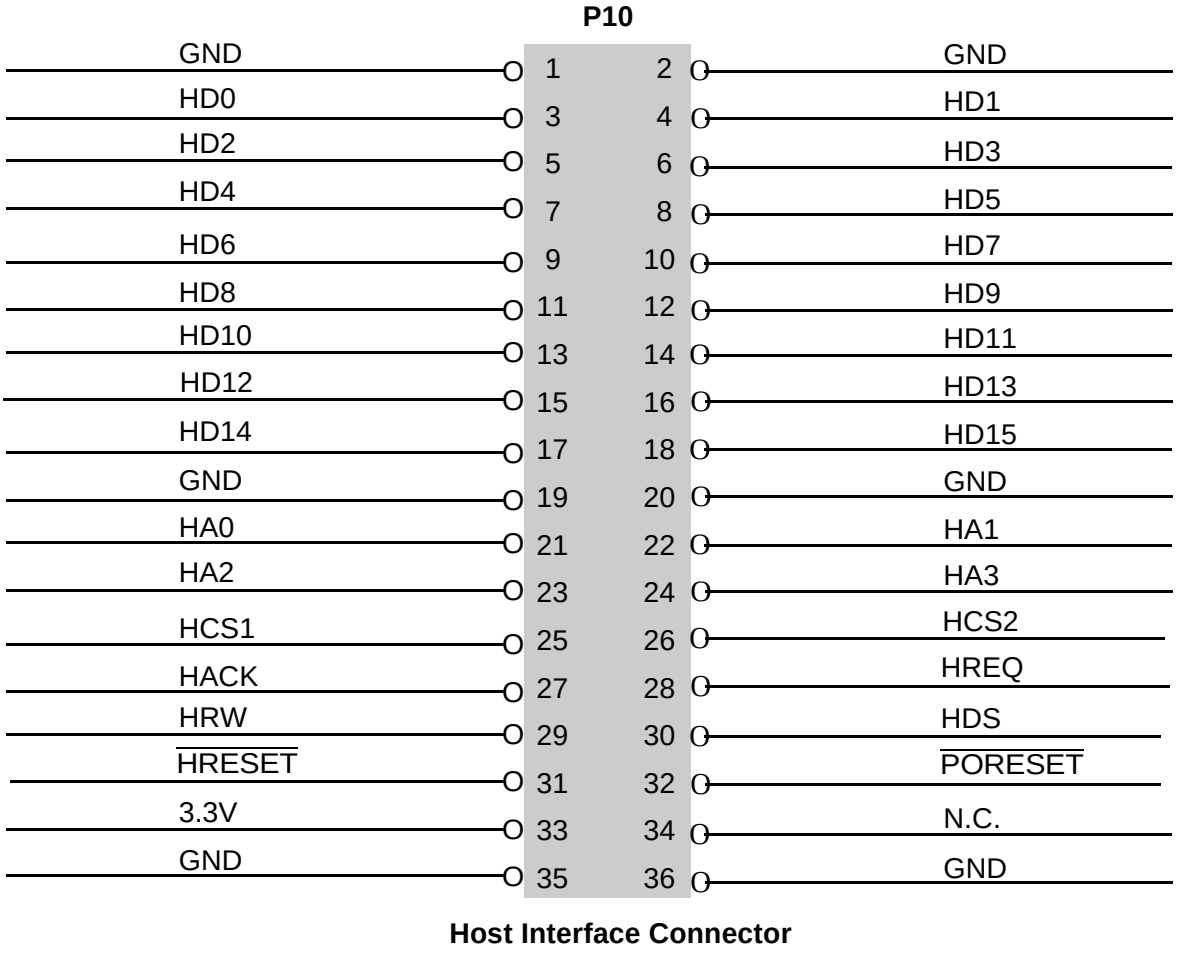


Figure 3-7. Host Interface Connector Signals

EVM Functional Description 4

This chapter discusses the MSC711xEVM block diagram and the functionality it describes. The design details of the various modules that make up the MSC711xEVM are described. This includes software initialization of the board.

4.1 MSC711xEVM Block Diagram

The MSC711xEVM block diagram is shown in **Figure 4-1**.

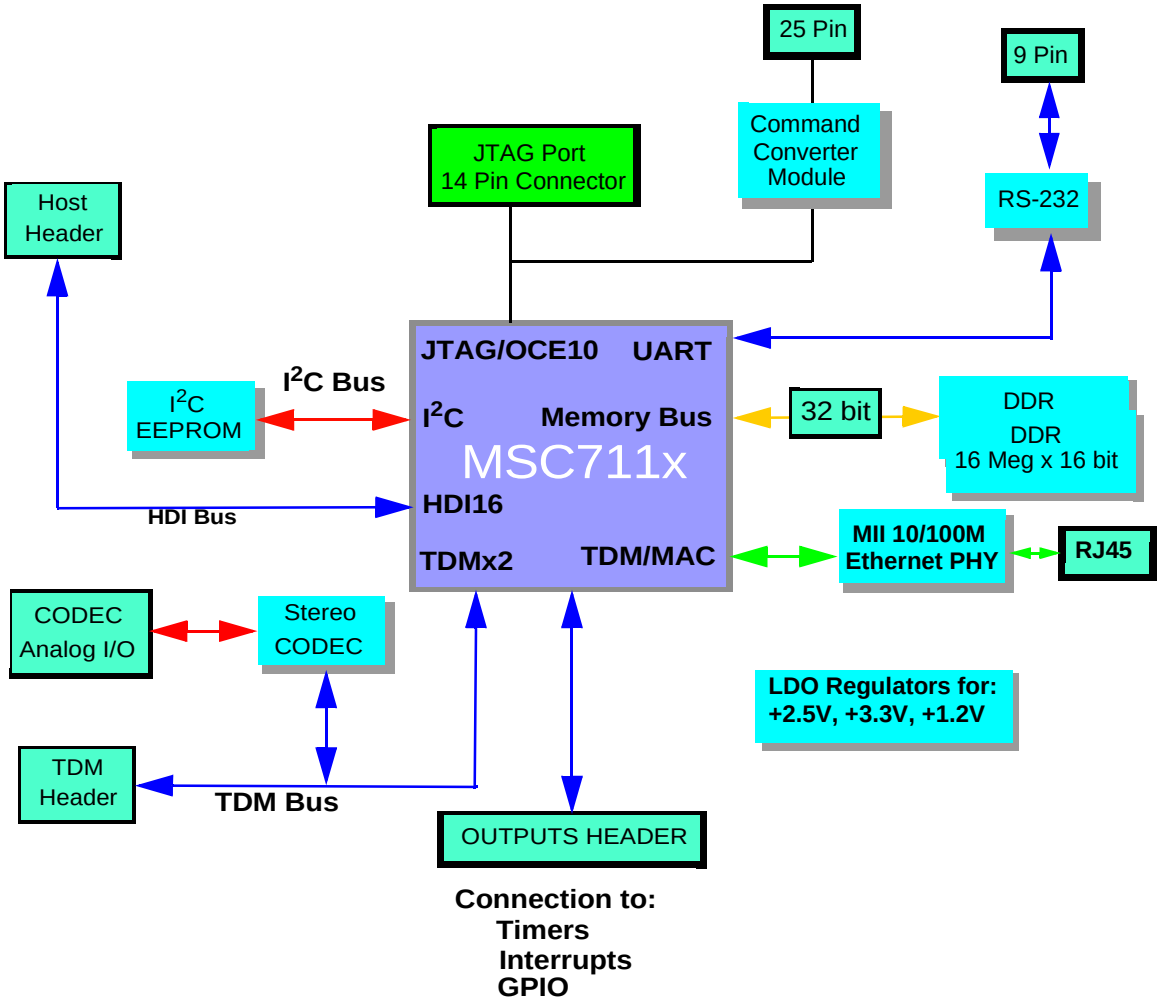


Figure 4-1. EVM Block Diagram

4.2 Reset and Reset-Configuration

There are several reset sources on the MSC711xEVM that generate two types of reset:

- MSC711x Power On Reset ($\overline{\text{PORESET}}$)
- MSC711x Manual Hard-Reset ($\overline{\text{HRESET}}$)

All MSC711xEVM reset sources are fed into the MSC711x reset controller, which takes different actions depending on the source of the reset, as shown in **Table 4-1**.

Table 4-1. Reset Sources

Reset Name	Source	Description
Power-On Reset ($\overline{\text{PORESET}}$)	Input	Initiates the PORESET flow that resets the EVM and configures various aspicts of the MSC711x.
Hard-Reset ($\overline{\text{HRESET}}$)	SW2	Initiates the hard reset flow that configures various attributes of the MSC711x device.
Software Watchdog Reset	Internal	A software watchdog reset is initiated when the watchdog count reaches zero. The enabled software event then generates an internal hard reset sequence ($\overline{\text{HRESET}}$).
Bus Monitor Reset	Internal	A bus monitor hard reset is asserted when the bus monitor count reaches zero. The enabled bus monitor event then generates $\overline{\text{HRESET}}$.
JTAG Commands	Internal	When an EXTEST, CLAMP or HIGHZ JTAG command executes, JTAG logic generates an internal soft reset sequence.

4.2.1 Power-On Reset

The power on reset to the MSC711x initializes the processor state after power up. The entire MSC711x device is reset. PLL and clock synthesis states are reset. $\overline{\text{HRESET}}$ is driven and the SC1400 core is reset. System configuration is sampled from SW3. Configuration pins are configured only at the deassertion of $\overline{\text{PORESET}}$.

A dedicated logic asserts $\overline{\text{PORESET}}$ input for a period long enough to include the MSC711x core voltages' stabilization, which are powered by a different voltage regulator.

4.2.2 Power-On Reset Configuration

At the rising edge of the Power-On signal, the MSC711x samples four pins to determine configuration. Those pins are BM0, BM1, SWTE and DBREQ. These are sampled only once after power-on reset.

Table 4-2. Pwer-On Reset Configuration

Signal	Description	Settings
BM1 - BM0	**Boot Mode:** (SW3 - subswitches 3 and 4) Sampled on the rising edge of $\overline{\text{PORESET}}$, these lines determine the boot mode.	0 - Boot from HDI16 port 1 - Boot from I^2C 2 - Reserved 3 - Reserved
SWTE	**Software Watchdog Timer Enable:** (SW3 - subswitch 2) Sampled on the rising edge of $\overline{\text{PORESET}}$, this bit vlaue can override the timer functionality.	0 - Watchdog Timer disabled 1 - Watchdog Timer enabled
DBREQ	**Debug Request:** (SW3 - subswitch 1)	

4.2.3 Hard Reset

Hard-Reset ($\overline{\text{HRESET}}$) signal may be generated on the EVM at the following sources:

- COP/JTAG Port
- OCE10/JTAG Port
- Manual Hard-Reset (SW2)
- Software Watchdog Reset
- Bus Monitor Reset

Hard-Reset, when generated, causes the MSC711x to reset all its internal hardware except for PLL logic and reacquire the hard-reset configuration from its current source. Since hard-reset resets also the refresh logic for dynamic RAMs, their content is lost as well.

$\overline{\text{HRESET}}$ is an open-drain signal and must be driven with an open-drain gate whenever an external source is driving it. Otherwise, contention will occur over that line, which might cause permanent damage to either board logic and/or to the MSC711x.

4.2.4 External Port Hard Reset

To provide convenient hard-reset capability for an OCE10/JTAG controller, an $\overline{\text{HRESET}}$ line appears at the OCE10/JTAG port connector. The COP/JTAG controller may directly generate hard-reset by asserting (low) this line. This $\overline{\text{HRESET}}$ effects only the MSC711x.

4.2.5 Manual Hard Reset

To allow run-time hard-reset on the EVM, manual $\overline{\text{HRESET}}$ is facilitated. The MSC711x has its own $\overline{\text{HRESET}}$ push-button (SW2).

4.2.6 Internal Sources Hard Reset

The MSC711x has two internal sources that can generate $\overline{\text{HRESET}}$ due to specific events:

- Software Watchdog Timer Reset
- Bus Timeout Monitor Reset

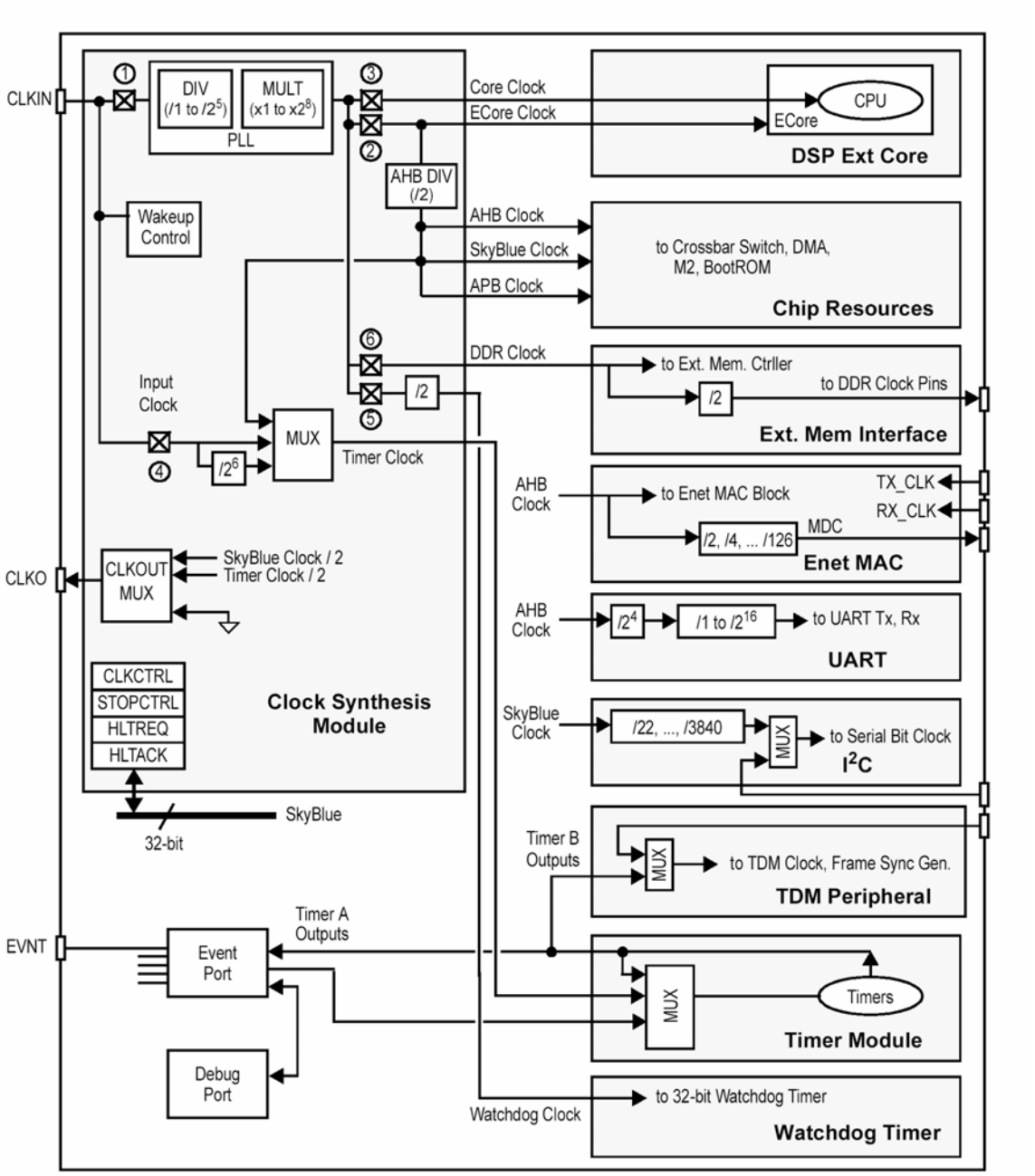
4.3 EVM Clock

The following paragraphs describe clocking on the MSC7116EVM. There are three main clock circuits on board:

- MSC711x System Clock (20MHz).
- CODEC clock (8.192MHz).
- CPLD clock (40MHz).

The MSC711x chip requires a reference clock input (CLKIN). From this clock input the internal clock synthesis module at the MSC711x core generates all the timing needs of the chip. The recommended CLKIN frequency is 20MHz.

The MSC711xEVM timing system is shown in **Figure 4-2**.



① Clocks can be disabled at this point in Stop mode — disables PLL, Core Clock, ECore Clock, AHB Clock, SkyBlue Clock, and APB Clock.
② Clocks can be disabled at this point in Stop mode — disables ECore Clock, AHB Clock, SkyBlue Clock, and APB Clock.
③ Clocks are disabled at this point in Wait and Stop modes — disables Core Clock.
④ Clocks can be disabled at this point in Stop mode — disables Input Clock used in Timer Clock Generation.
⑤ Clocks can be disabled at this point in Stop mode — disables Watchdog Timer Clock.
⑥ Clocks can be disabled at this point in Stop mode — disables DDR Clock.

Figure 4-2. EVM Timing System

The MSC711x timing system has the clock synthesis module at its core. This module is composed of the following blocks:

- Phase lock loop (PLL) with associated multipliers and dividers
- AHB Bus Clock Divider
- APB Bus Clock Divider
- Timer Clock MUX
- Wakeup Control
- Control registers

Together, these blocks generate the clock signals used for core and peripheral clocking. An external input clock input provides a reference clock for the system.

The Core Clock is obtained by a pre-division of the input clock and multiplying the frequency in the PLL. The AHB clock is generated in a manner similar to the core clock, but with an additional division stage.

The SkyBlue clock is generated from the AHB clock. The APB clock is generated from the AHB clock. The timer clock can be derived from the external input clock or from the SkyBlue clock.

The control register is used for programming the clock synthesis module. The wakeup control block is used for waking the chip out of its low power modes.

4.4 TDM Interface and Stereo Codec

The MSC711x chip has 3 TDM ports: TDM0,TDM1 and TDM2.

The TDM2 port uses BI functional pins with the ETHERNET port and cannot be used if the ETHERNET port is working (in MII MODE).

The TDM0 port is used in the MSC711x_EVM board to connect to the AKM stereo codec (AK4554 or AK4550). The codec can sample the analog input stereo signal at a variable sampling rate that is determined automatically by the combination of 3 input clocks that are provided to the codec. For details, see the AKM AK4554 Codec Data Sheet in the system clock input section.

The MSC711x_EVM board has a 8.192MHz oscillator that is connected to pin EVENT0 in the MSX711x chip, This is the input for the Timer module that can divide the basic 8.192MHz frequency to 4.096MHz and 2.048MHz and bring it back to pin EVENT1 that is connected to the Master Clock pin at the codec (MCLK). For details, see **Figure 4-2** and the schematics in Appendix A.

This gives the user the option to decide the codec sampling rate frequency (32KHz , 16KHz or 8KHz), or to determine another frequency according to the divider in the MSC711x timer unit.

4.5 I2C Boot EEPROM

The MSC711x device can be booted from the HDI16 BUS or from external EEPROM with serial I2C interface. In the MSC711xEVM a serial EEPROM device such as the M24256-B from STmicroelectronics Co. is used. The memory of this standard 256KBit device is organized as 32Kx8. The device has the capability of hardware write-protecting its memory map. The device is fitted into an EVM socket to make it capable of being reprogrammed by an external programmer. Other replacement chips for the EVM serial I2C EEPROM are:

- Microchip 24LC256.
- ATMEL AT24C256.
- CATALYST CAT24WC256.

4.5.1 EVM EEPROM Operation

Visual indication of the EVM SCL and SDA line status is provided by corresponding Red and Green LED's (LDx and LDx, respectively). The I2C bus is connected to a two test points header.

The I2C EEPROM address is set to "000". The serial EEPROM I2C Bus clock is 400KHz.

4.5.2 EVM EEPROM Summary Description

The I2C compatible electrically erasable programmable read-only memory (EEPROM) device (M24256-B) is organized as 32K x 8 bits, as shown in .

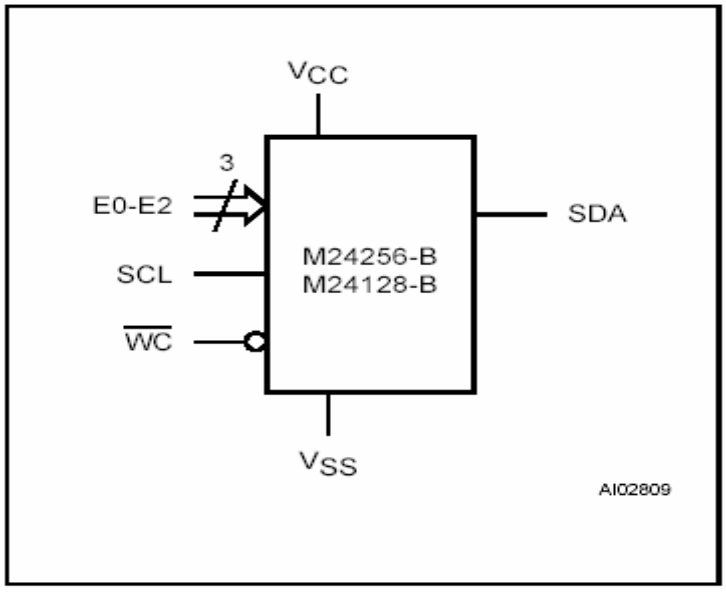


Figure 4-3. I2C EEPROM Description

I^2C EEPROM device pins are described in **Table 4-3**.

Table 4-3. EEPROM Device Pins and Signals

Pin	Signal
E0, E1, E2	Chip Enable
SDA	Serial Data
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

These devices are compatible with the I^2C memory protocol. This is a two wire serial interface that uses a bi-directional data bus and serial clock. The memory carries a built-in 4- bit unique Device Type Identifier code (1010) in accordance with the I^2C bus definition.

The memory behaves as a slave device in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the bus master. The START condition is followed by a Device Select Code and RW bit, as described in **Figure 4-4**, terminated by an acknowledge bit.

	Device Type Identifier				Chip Enable			$R\overline{W}$
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select Code	1	0	1	0	0	0	0	$R\overline{W}$

Note: 1. The most significant bit, b7, is sent first.

Figure 4-4. Device Select Code

When writing data to the memory, the memory inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission.

When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a STOP condition after an Ack for WRITE, and after a No Ack for READ.

4.6 JTAG/OCE10

The JTAG /OCE10 test access port (TAP) connection, command converter and I^2C Boot EEPROM are detailed in the block diagram represented in **Figure 4-5**.

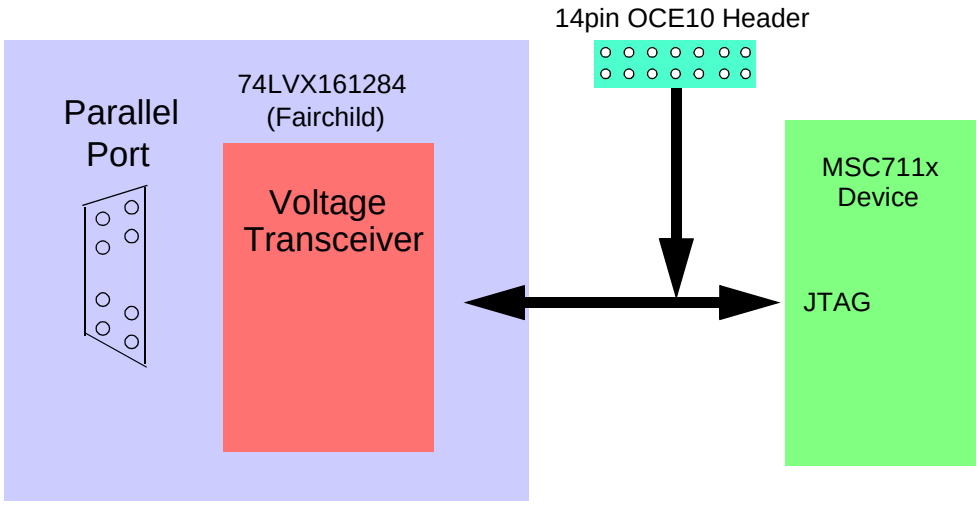


Figure 4-5. Parallel Port Connection (JTAG)

4.6.1 JTAG TAP Connection

The OCE10's JTAG interface requires a test access port (TAP) controller that includes OCE-10 -specific logic and support for three OCE-10-specific JTAG instructions. The JTAG connection on the MSC711x device can be provided via two ways:

- Direct connection to the appropriate header connector.
- Optional Host PC Parallel Port connection.

4.6.2 JTAG/OCE10 Header

The JTAG header provides connection between the MSC711x device and any external compatible JTAG converter such as a Wiggler etc.

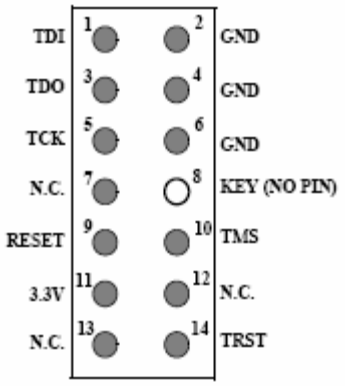


Figure 4-6. JTAG/OCE10 Port Connector

Pins and signals of the the JTAG/OCE10 header are described in **Table 4-4**.

Table 4-4. JTAG/OCE10 Header Pinout

Pin No.	Signal	Attribute	Description
1	TDI	I	Transmit Data In. This is the JTAG serial data input of the ADS, sampled on the rising edge of TCK.
2	GND	P	Digital Ground. Main GND plane.
3	TDO	O	Transmit Data Output. This the MSC711x JTAG serial data output driven by Falling edge of TCK.
4	GND	P	Digital Ground. Main GND plane.
5	TCK	I	Test port Clock. This clock shifts in / out data to / from the MSC711xEVM JTAG logic. Data is driven on the falling edge of TCK and is sampled both internally and externally on it's rising edge. TCK is pulled up internally by the MSC711x.`
6	GND	P	Digital Ground. Main GND plane.
7	N.C.	-	Not Connected.
8	KEY	-	No pin in connector. Serve for correct plug insertion. Not Connected.
9	$\overline{\text{RESET}}$	I/O, P.U.	In fact, $\overline{\text{HRESET}}$. When asserted by external H/W, generates Hard-Reset sequence for the MSC711x. During that sequence, asserted by the MSC711x. for 512 system clocks. Pulled Up on the EVM using a 10K pullup. ***Caution:*** *When driven by an external tool, this signal MUST be driven with an Open Drain gate. Failure to do so might result in permanent damage to the MSC711x and / or to EVM logic.*
10	TMS	I	Test Mode Select. This signal, qualified with TCK in a same manner as TDI, changes the state of the JTAG machines. This line is pulled up internally by the MSC711x.
11	VDD	P	Connect to 3.3V power supply bus. May be used for Command Convertor power.
12	N.C.	-	Not Connected
13	N.C	-	Not Connected
14	$\overline{\text{TRESET}}$	I	Test Port Reset. When this signal is active (Low), it resets the JTAG logic of the MSC711x. This line is pulled-down on theEVM with a 1K resistor, to provide constant reset of the JTAG logic.

4.6.3 Parallel Port Connection

The MSC711xEVM is connected to the host PC parallel port via an on board JTAG converter operating in SPP mode.

4.6.4 JTAG Operational LED LD7

On the EVM, LD7 indicates the current JTAG operation.

When LD7 is lit, a parallel port cable is not attached to the EVM board. The user can connect to the board using a third company external device via the OCE10/JTAG connector (P9).

When the parallel cable is connected at P1, LD7 turns off and communication is made by an internal device.

4.7 DDR SDRAM Interface

The External Memory Interface in the MSC711x has the following characteristics:

- Page-mode DDR-RAM machine.
- Glueless interface to 100 MHz 14-bit page mode DDR-RAM.
- 64 MByte external address space (14-bit external address bus with 4 banks).
- 16-bit or 32-bit external data bus.

The MSC711xEVM uses a 32 bit external data bus. The most common DDR SDRAM device chip @16bit is 16M x 16bit = 256Mbit. Therefore, for the MSC711xEVM uses 2 DDR chips. The devices to be used are:

- MICRON: MT46V8M16
- HYNIX :HY5DU281622ET

4.7.1 SSTL_2 Interface

Previous SDR memory technology used LVTTL and a fixed voltage level for its signal interface. DDR SDRAM utilizes differential inputs and a reference voltage for all interface signals. This interface is called SSTL_2, which stands for “Stub Series Terminated Logic for 2.5 volts”.

The benefits of the SSTL_2 interface include symmetrical low and high logic levels, improved signal integrity and better noise immunity.

4.7.2 SSTL_2 Signals and Line Termination

The typical SSTL_2 interface includes series termination and a pull-up to the termination voltage (refer to Figure 6 1 : Typical SSTL_2 interface, with active termination.). The SSTL_2 interface uses a reference voltage and differential input to determine the logic levels. The reference voltage is defined to be half of the supply voltage and the termination voltage equals the reference voltage. (VDD = 2.5 volts, VREF = VTT = 1.25 volts).

This is an active termination, as shown in **Figure 4-7**.

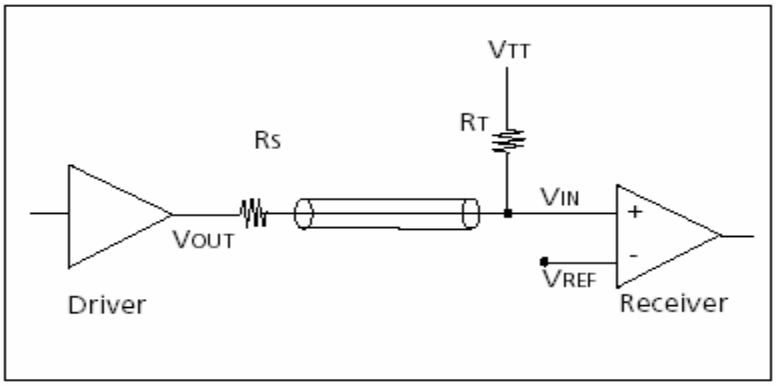


Figure 4-7. Typical SSTL_2 Interface

4.7.3 MSC711x_EVM DDR Connection

In the bi-directional data bus there is a problem because the source is changing all the time. The solution is to locate the MSC711x and the DDR chip as close as possible on the board and to put the termination resistor between them. The MSC711xEVM DDR Connection is shown in **Figure 4-8**.

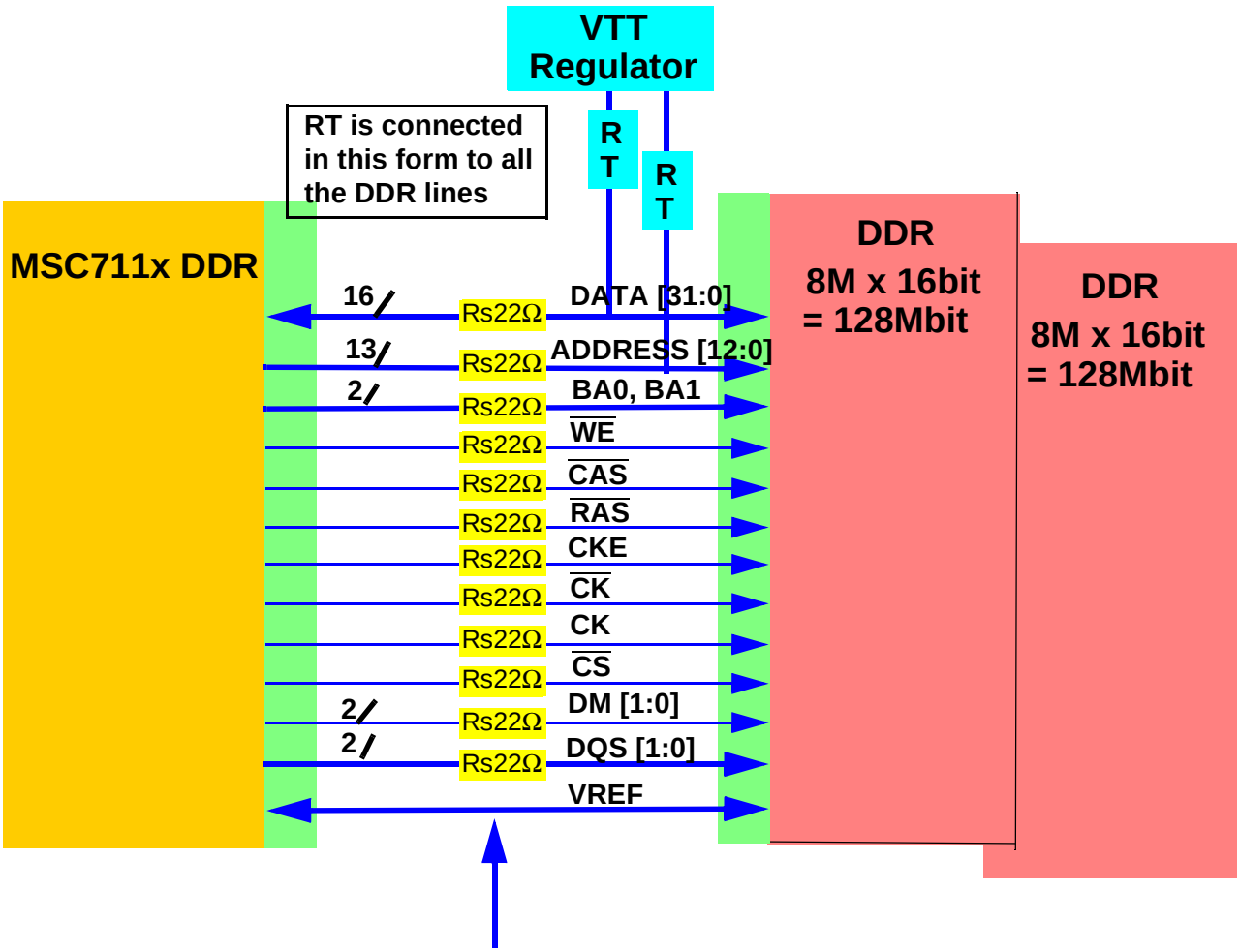


Figure 4-8. DDR - MSC711x Connection

4.8 Fast Ethernet (10/100 Base-T)

A Fast Ethernet port 10/100-Base-T I/F is provided on the MSC7116_EVM. The Ethernet PHY used on the MSC7116_EVM is VT6103 by VIA. This is a physical layer single-chip transceiver for 100BASE-TX and 10BASE-TX operations.

The VT6103 connects to the Medium Access Control (MAC) layer through the Media Independent Interface (MII). The MSC711x port can be switched between 2 Ethernet modes: MII and RMII. But on the MSC711x_EVM only the MII mode is used.

The VT6103 uses a low power and high performance CMOS process. It contains the entire physical layer function of 100BASE-TX, as defined by IEEE802.3u. The VT6103 provides support for the auto-negotiation function, utilizing automatic media speed and protocol selection.

The magnetic used in the MSC7116_EVM is H1265 from PULSE. But there are another vendors for this magnetic, like Traxcom TRC88515.

The Fast Ethernet and Ethernet schemes are shown in **Figure 4-9**.

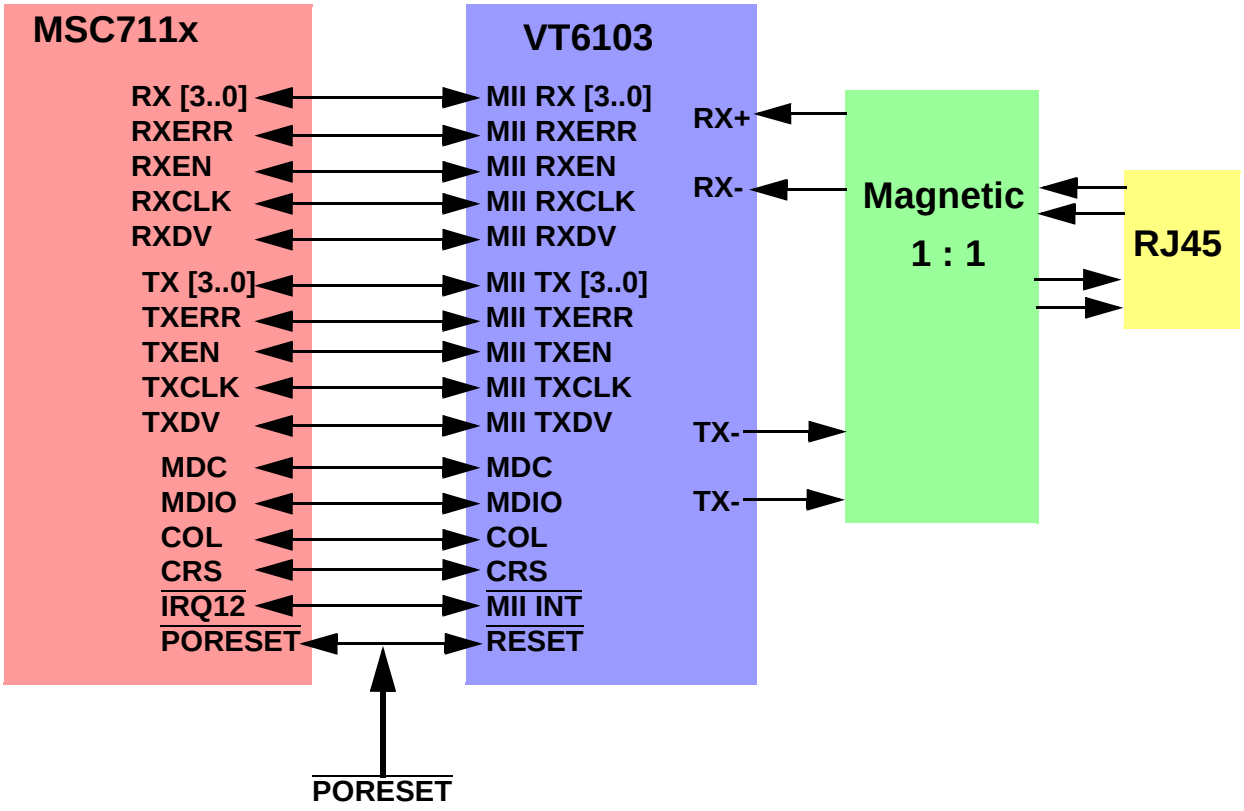


Figure 4-9. EVM Fast Ethernet and Ethernet

4.8.1 VT6103 Control

The VIA VT6103 ETHERNET PHY is controlled via a 2 wire interface: a clock (MDC), and a bidirectional data line (MDIO). This is in fact a bus, i.e., up to 32 devices may reside on it,. The protocol defines a 5-bit slave address field, which is compared with the slave address assigned to each device by hardware during device reset, according to the levels on some pins.

The MPC interfaces this port using the following two pins:

- MII_MDIO for MDIO.
- MII_MDC for MDC.

The MDIO port may interrupt a host in 2 ways: by driving low the MDIO line during IDLE time, or by using a dedicated interrupt line. This line (MDINT) is connected to the MSC711x IRQ X line in Fast Ethernet I/F and IRQ XX line in Ethernet I/F. It appears also at the expansion connectors.

EVM Memory Maps and Bus Mapping 5

5.1 Memory Controllers

The MSC711xEVM memory controller supports an interface to external memory and peripheral devices on the system bus and enables interfacing with the HDI16 bus.

The MSC711x memory controller provides a glueless interface between the internal MSC711x bus and the external double data rate (DDR) SDRAM memory modules. It establishes this interface by translating internal bus accesses to the appropriate address, data and control signals for DDR SDRAMs.

5.2 Memory Maps

The MSC711x memory maps are discussed in the following sections. Both On and Off chip address space is discussed, although the Off chip address space is used for the DDR only. The memory maps defined in the following tables are only a recommendation. Users may choose to work with alternative memory mapping. The described mode is supported by Metrowerks' CodeWarrior debug tool.

5.2.1 Extended Core Memory 1

When accessed by the SC1400 core, the MSC711x extended core memory address range is shown in **Table 5-1**.

Table 5-1. Extended Core Memory (M1)

Address Range	Description	Size
01800000 - 0182FFFF	M1 memory, when accessed by the SC1400 core	192 KB
01830000 - 01F7FFFF	Reserved	—

5.2.2 Extended Core Registers (ICache Array)

The MSC711x extended core register map is shown in **Table 5-2**.

Table 5-2. Extended Core Registers, ICache Array

Address Range	Description	Size
00EFF000 - 00EFFFFF	OCE10 Registers	—
00F00000 - 00F1FFFF	Instruction Cache Registers Extended Core Interface Registers	—
00F20000 - 00F23FFF	ICache Array Contents	16 KB
00F24000 - 00FFFFFF	Reserved	—

5.2.3 On-Chip Memory Outside Platform (M2, Boot ROM)

The MSC711x outside platform on-chip memory map is shown in **Table 5-3**.

Table 5-3. On-Chip Memory, M2 Boot ROM

Address Range	Description	Size
01000000 - 0102FFFF	M2 Memory	192 KB
01030000 - 013FFFFF	Reserved	—
01400000 - 01401FFF	Boot ROM	8 KB
01402000 - 017FFFFF	Reserved	—

5.2.4 Extended Core Memory - 2

When accessed by the DMA (using the ADDMA bus), or accessed by the Ethernet MAC (using the AMENT bus), the address range of the MSC711x extended core M1 memory is shown in **Table 5-4**.

Table 5-4. Extended Core Memory (M1)

Address Range	Description	Size
00000000 - 0002FFFF	M1 memory, when accessed by the DMA (using the ADDMA bus) or by the Ethernet MAC (using the AMENT bus).	192 KB
00030000 - 00EFFDFF	Reserved	—

5.2.5 Peripherals

You can access peripherals outside the platform using the ASTH, ASSB, and ASAPB buses at the following address ranges, as shown in **Table 5-5**.

Table 5-5. Peripheral Access

Address Range	Description	Size
01F80000 - 03FFFFFF	TDM / HDI16 high speed ports (via ASTH bus)	—
04000000 - 05FFFFFF	IPBus peripheral registers (via ASSB bus)	32 KB
06000000 - 07FFFFFF	APB peripheral registers (via ASAPB bus)	32 KB

5.2.6 Off-Chip Address Space

You can access off chip memory (DDR memory) using the ASEMI bus at the following address ranges, as shown in **Table 5-6**.

Table 5-6. DDR Memory Access

Address Range	Description	Size
08000000 - 1FFFFFFF	Reserved	—
20000000 - FFFFFFFF	External DDR memory (via ASEMI bus)	—

5.3 Host Processor Interface (HDI16)

The host processor (outsider host) is connected to the MSC711x chip through the HDI16 bus, via the EVM's 36 pin male header P10. The host interface (HDI16) in the MSC711x chip is a 16-bit wide, full-duplex, double-buffered parallel port that can directly connect to the data bus of a host processor.

The HDI16 port in the MSC711x supports a variety of buses and gluelessly connects with a number of industry-standard microcomputers, microprocessors, and DSPs.

The HDI16 port is designed so that its host bus can be asynchronously accessed independent of the clocks on the chip. This is accomplished by dividing the HDI16 registers into two banks:

- "External Host register bank is accessible by an external host.
- "Chip register bank is accessible by the MSC711x device.

The HDI16 supports two classes of interfaces to external devices:

- "Host processor/Microcontroller (MCU) connection interface.
- "DMA controller interface.

5.3.1 HDI16 Configuration

On the MSC711x device, the HLEND bit in the HPCR register must always be "0", which configures the HDI16 module for big endian operation. This is the default value out of reset.

5.3.1.1 Special MSC711x HDI16 Port Characters

The HDI16 port on the MSC711x is different from the MSC8101 HDI16 port. The main differences lie in the following features:

- "Bits on HD bus are numbered with bit 0 as the LSB.
- "Bits on HA bus are numbered with bit 0 as the LSB.
- "Bits in HDI16 registers are numbered with bit 0 as the LSB.
- "The Host Port Pin (HPE)does not exist as a pin on the MSC711x. Instead this signal is internally tied as asserted, i.e., host port is enabled! (to disable this port use the HEN bit in the HPCR register).
- "HDSP pin value is sampled only on reset.
- "H8BIT pin value is sampled only on reset.
- "Host Address Bus uses only 3 pins HA[2:0], pin HA(3) is not in use, it is internally asserted to '0'.
- "The reset configuration registers are not accessible by an external host and are not supported.

5.3.1.2 HDI16 Bus Signals

The HDI16 bus carries the following signals:

- HD[15:0] host data bus (in 16-bit mode).
- HD[7:0] host data bus (in 8-bit mode).
- HA[2:0] host address lines .
- HRW/HRD read/write select (HRW) or read strobe (HRD).
- HDS/HWR data strobe (HDS) or write strobe (HWR).
- $\overline{\text{HCS1}}$ host chip-select 1.
- $\overline{\text{HCS2}}$ host chip-select 2.
- HREQ/HTRQ host request (HREQ) or host transmit request (HTRQ).
- HACK/$\overline{\text{HRRQ}}$ host acknowledge (HACK) or host receive request ($\overline{\text{HRRQ}}$).
- HDDS dual data strobe control input.

The HDI16 Bus connection to the host processor header are shown in**Figure 5-1** .

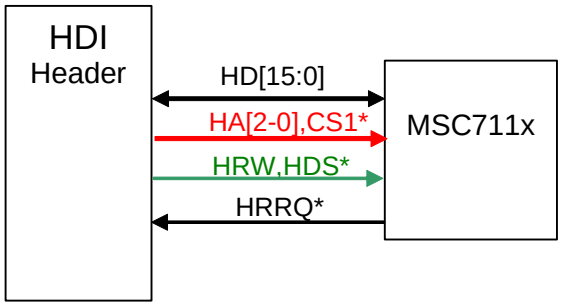


Figure 5-1. HDI16 Bus Connection to Header P10

The Host I/F connector (P10) is a 36 pin, two row, header connector. The connection between the MSC711xEVM board and the Host Board is by a 36 line flat cable. The pins and signals of connector P10 are shown in **Figure 5-2** and **Table 5-6**, respectively.

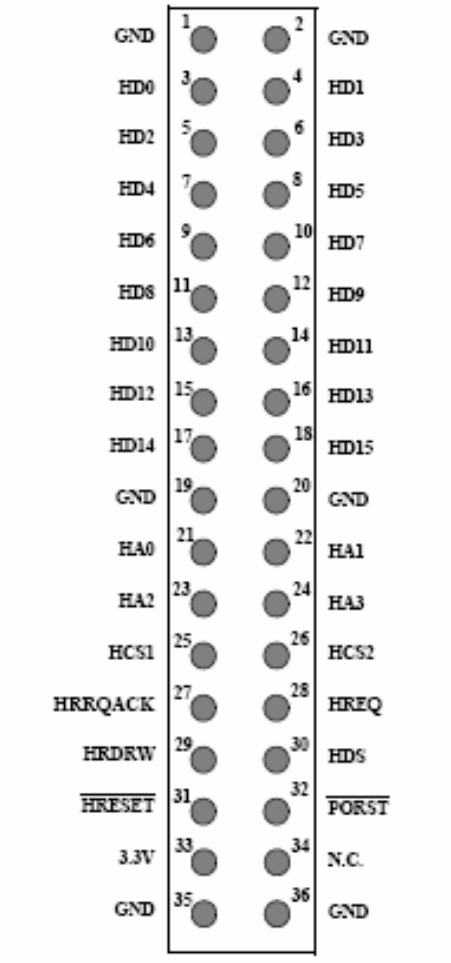


Figure 5-2. The Host I/F Connector.

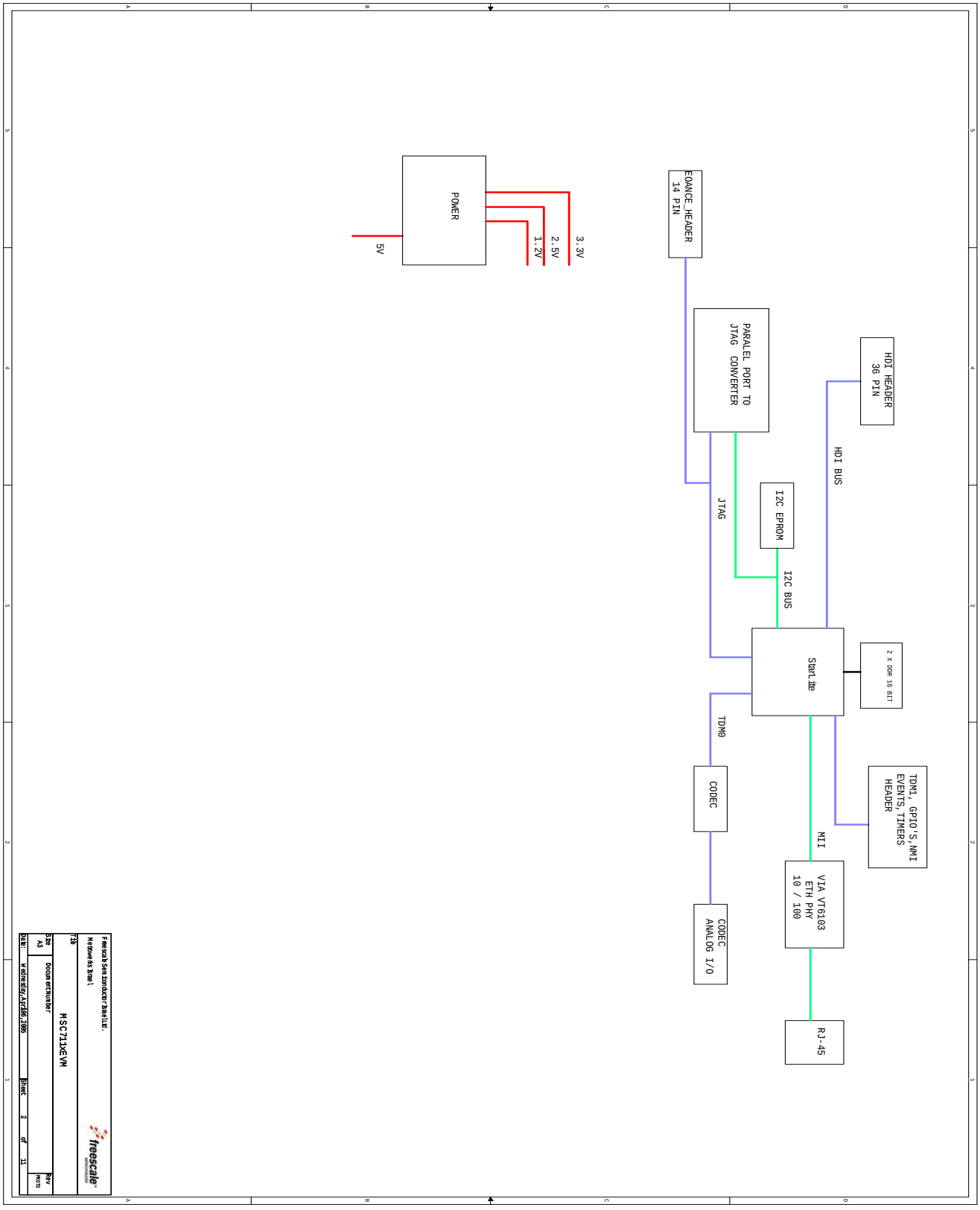
MSC711xEVM Schematics A

A.1 MSC711xEVM Schematics

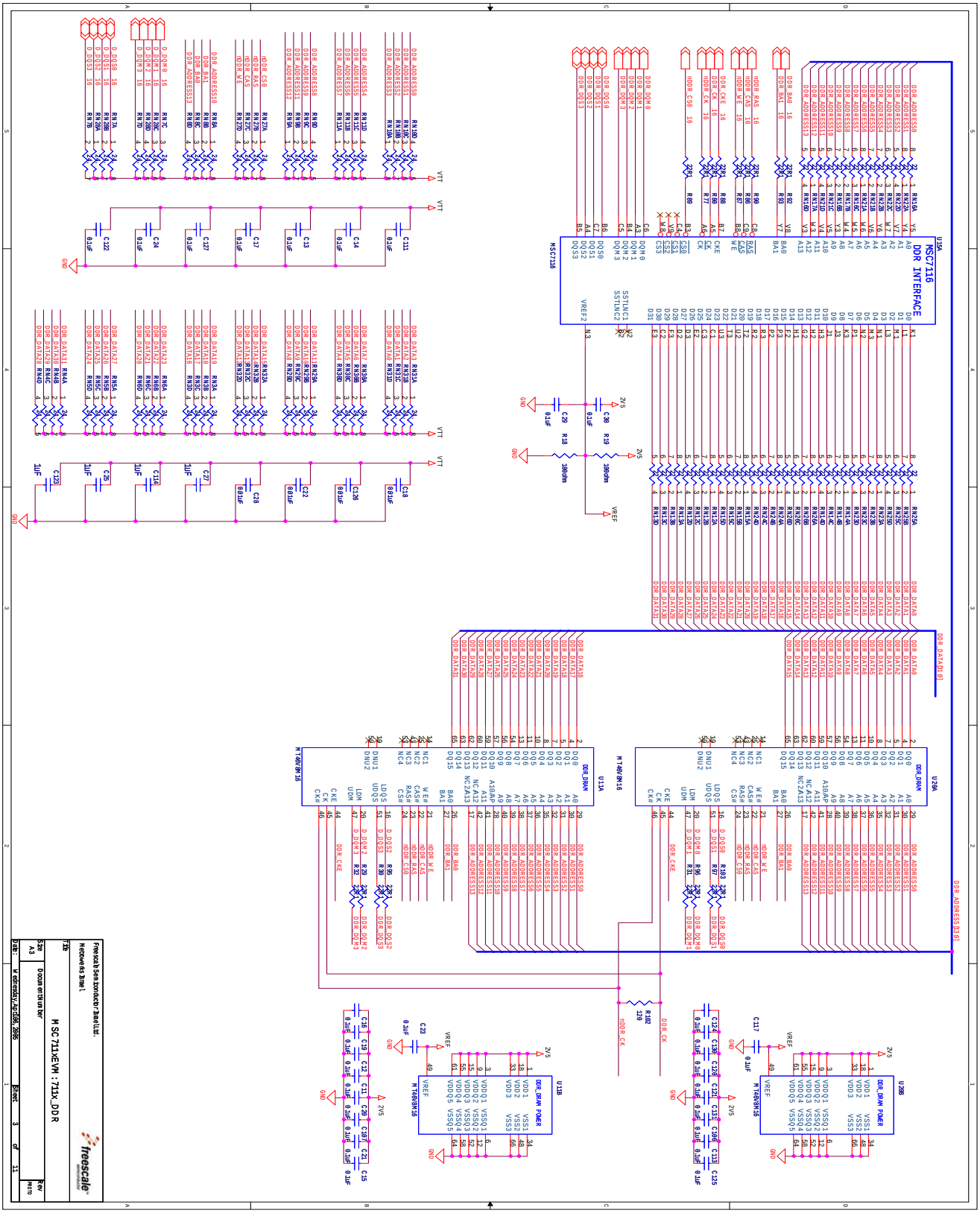
Schematics for the MSC711xEVM board can be seen on the following pages and are listed in **Table A-1**.

Table A-1. MSC711xEVM Schematics

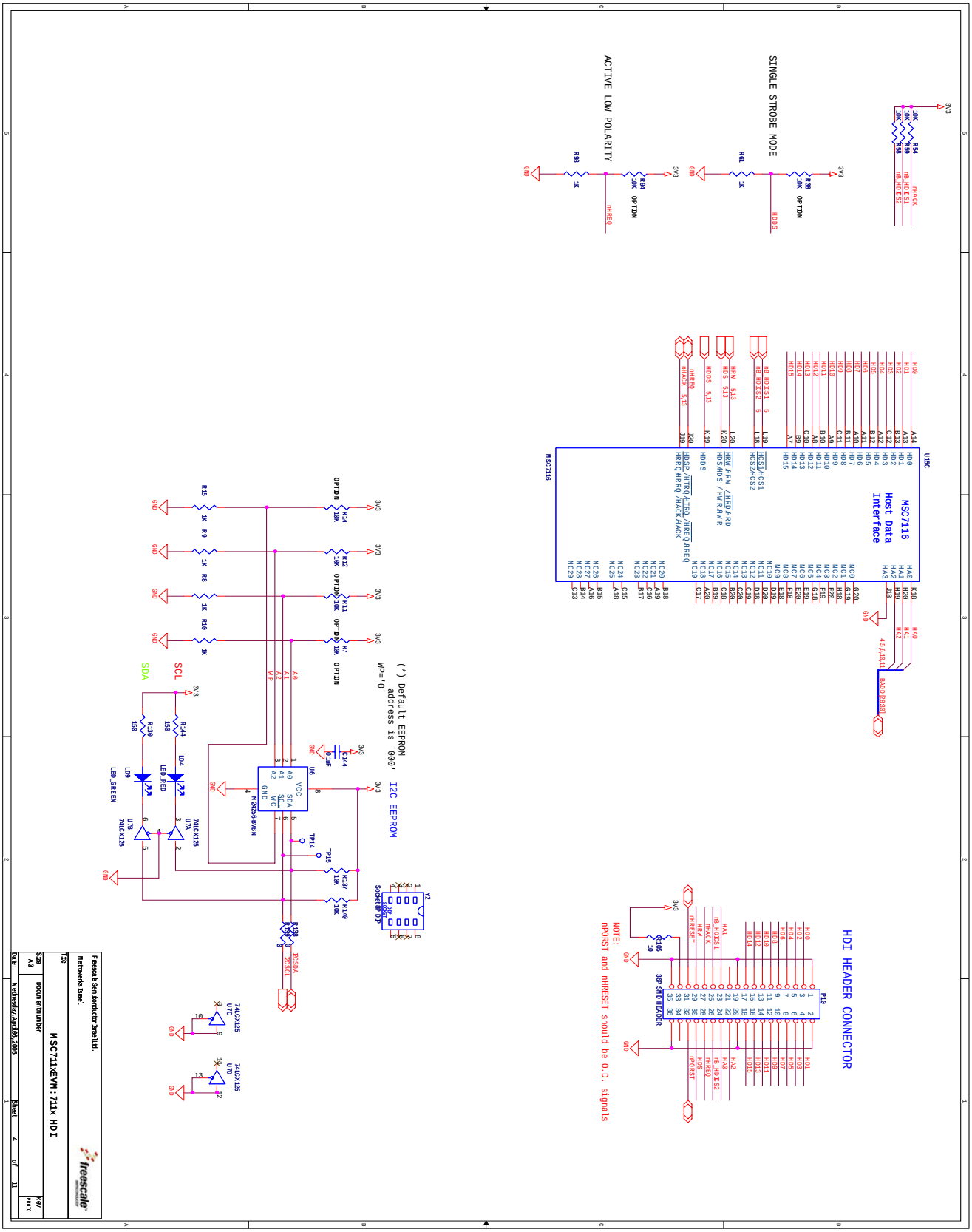
A.1.1 Block Diagram



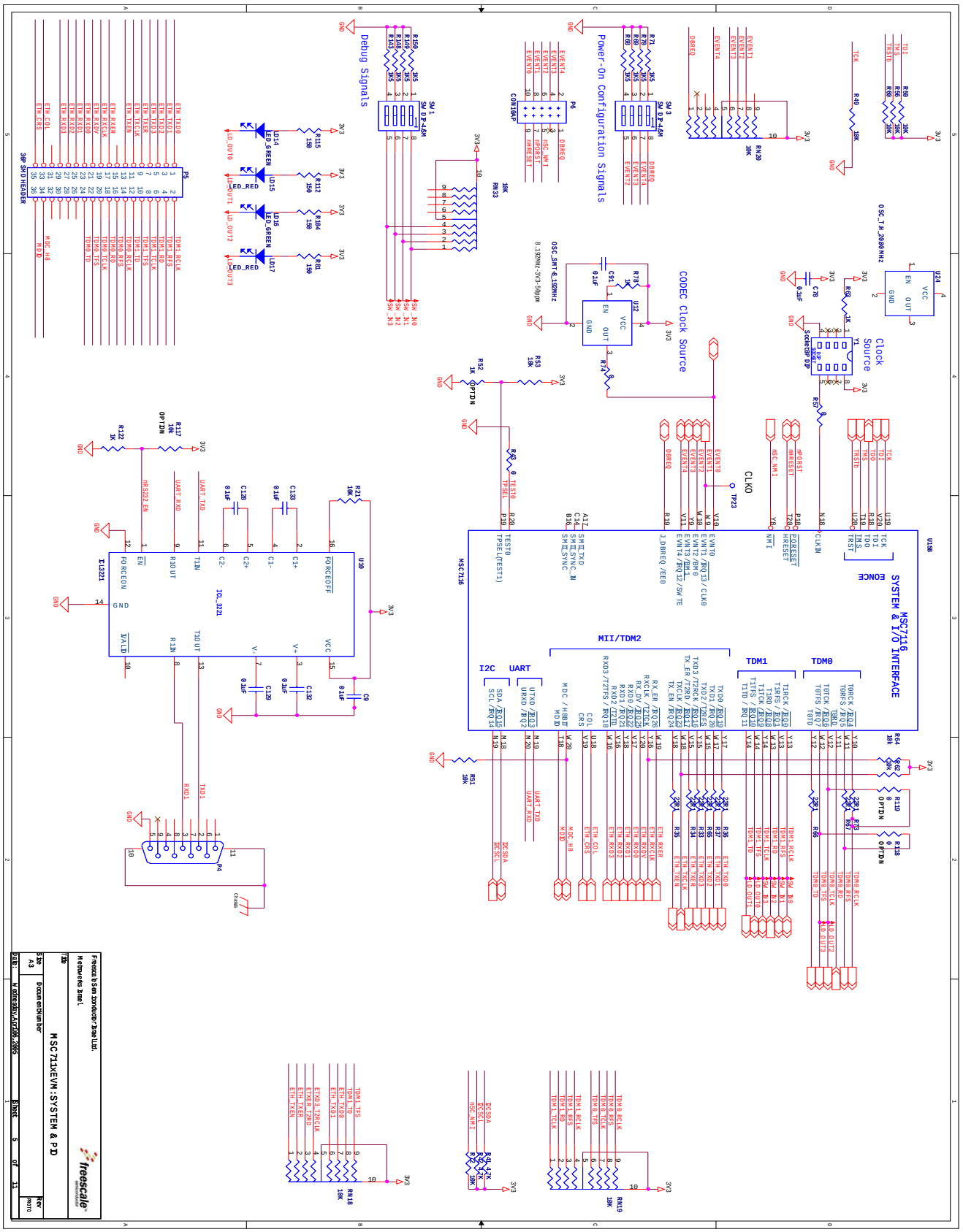
A.1.2 StarLite DDR



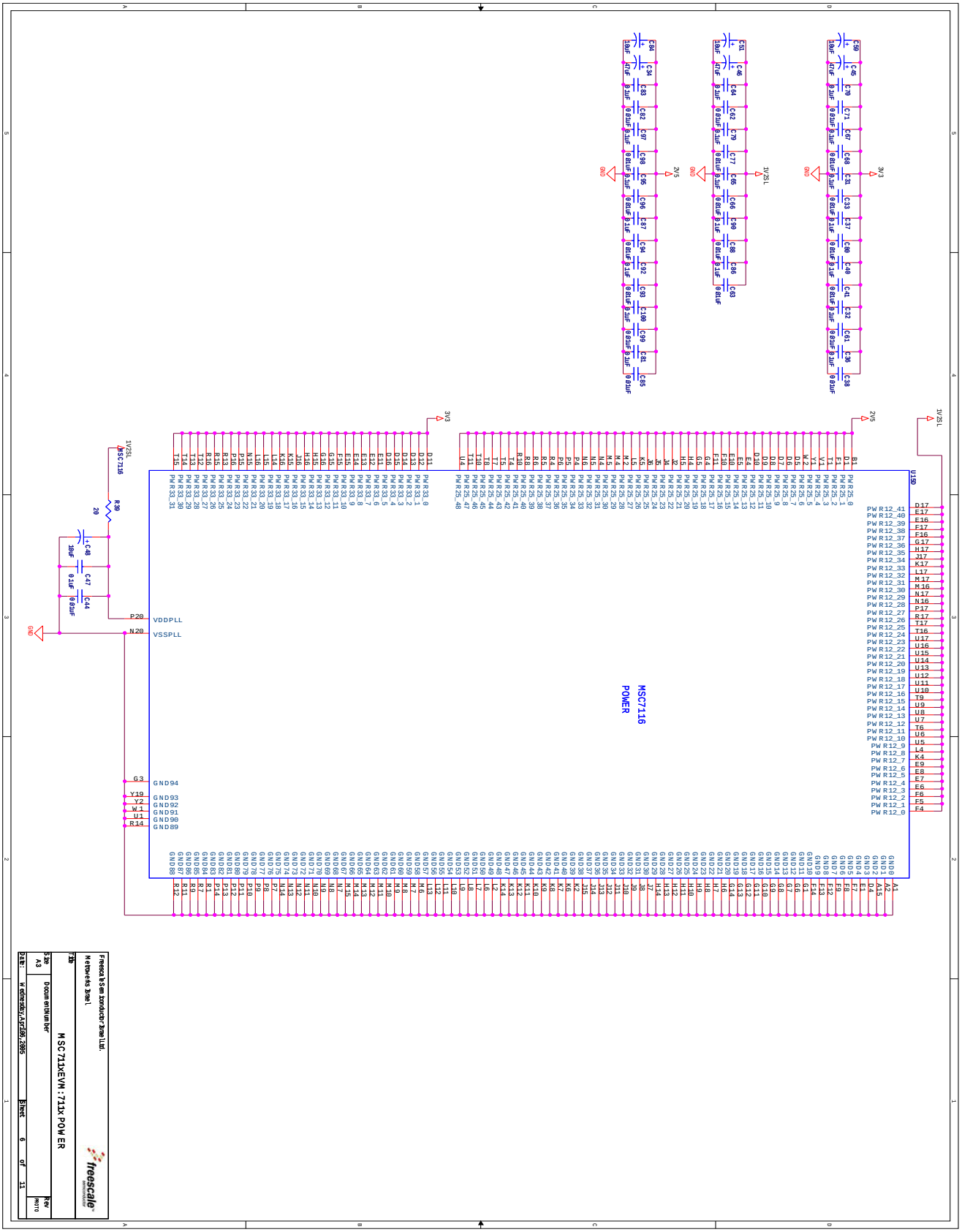
A.1.3 StarLite HDI



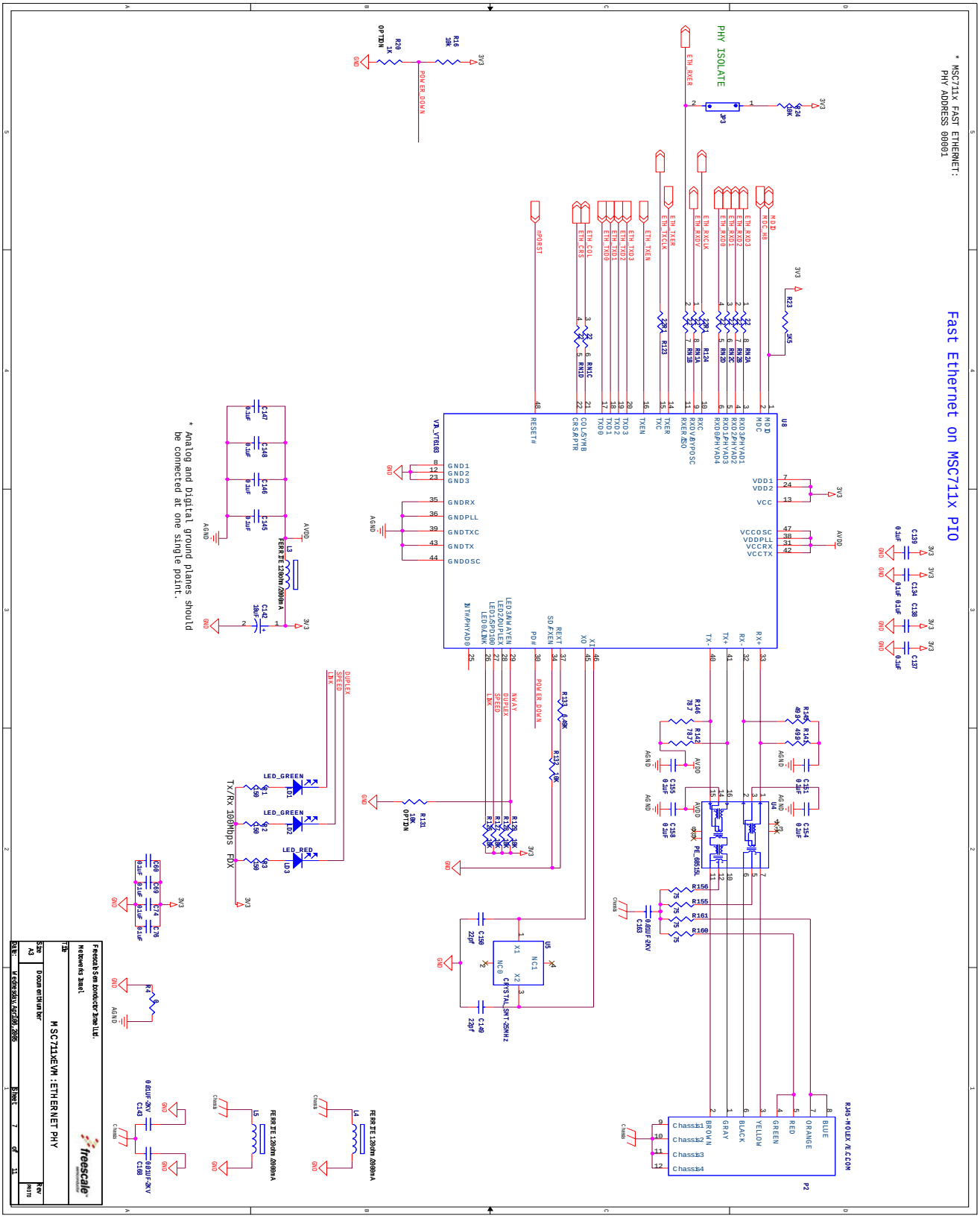
A.1.4 StarLite System and PIO



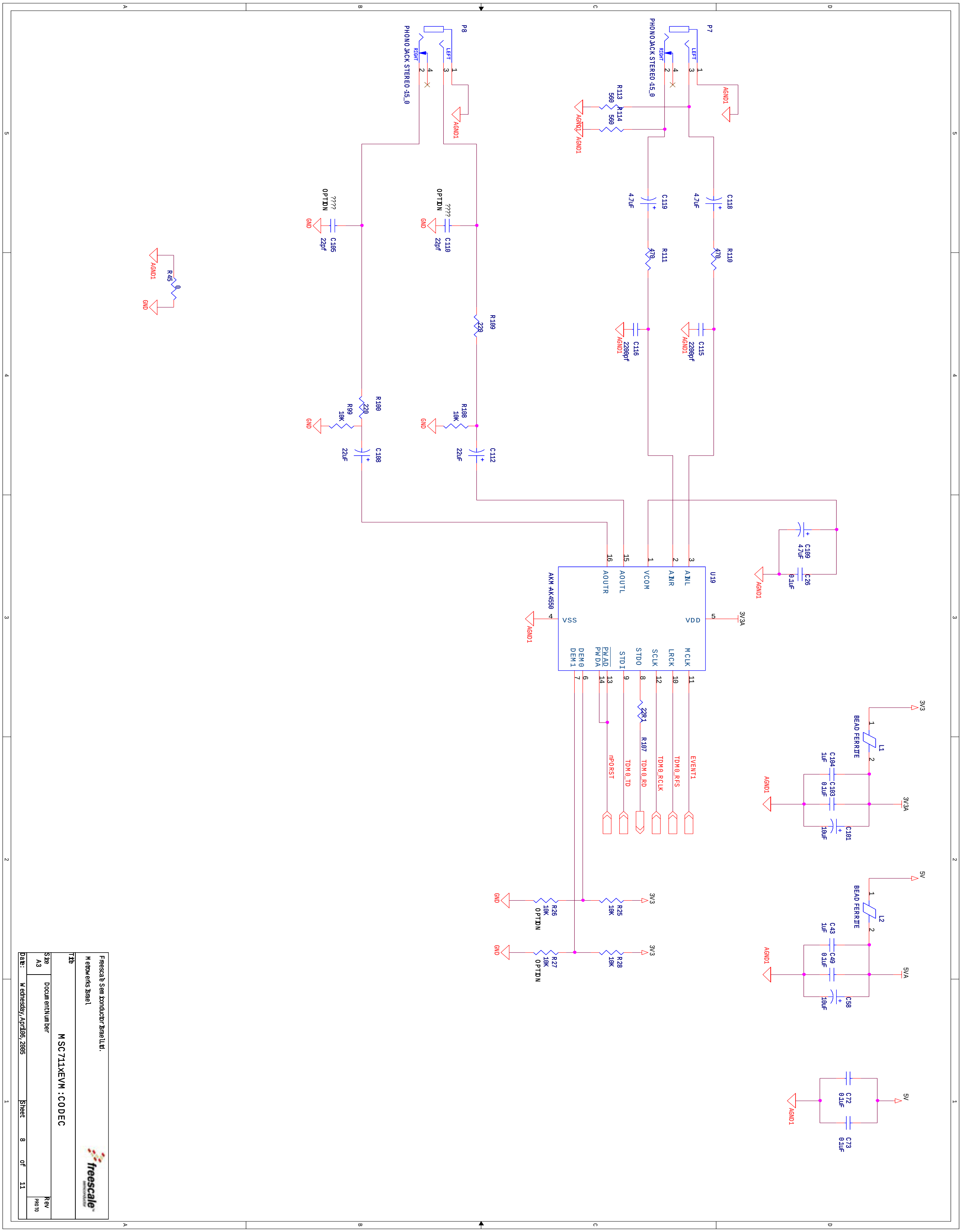
A.1.5 StarLite Power



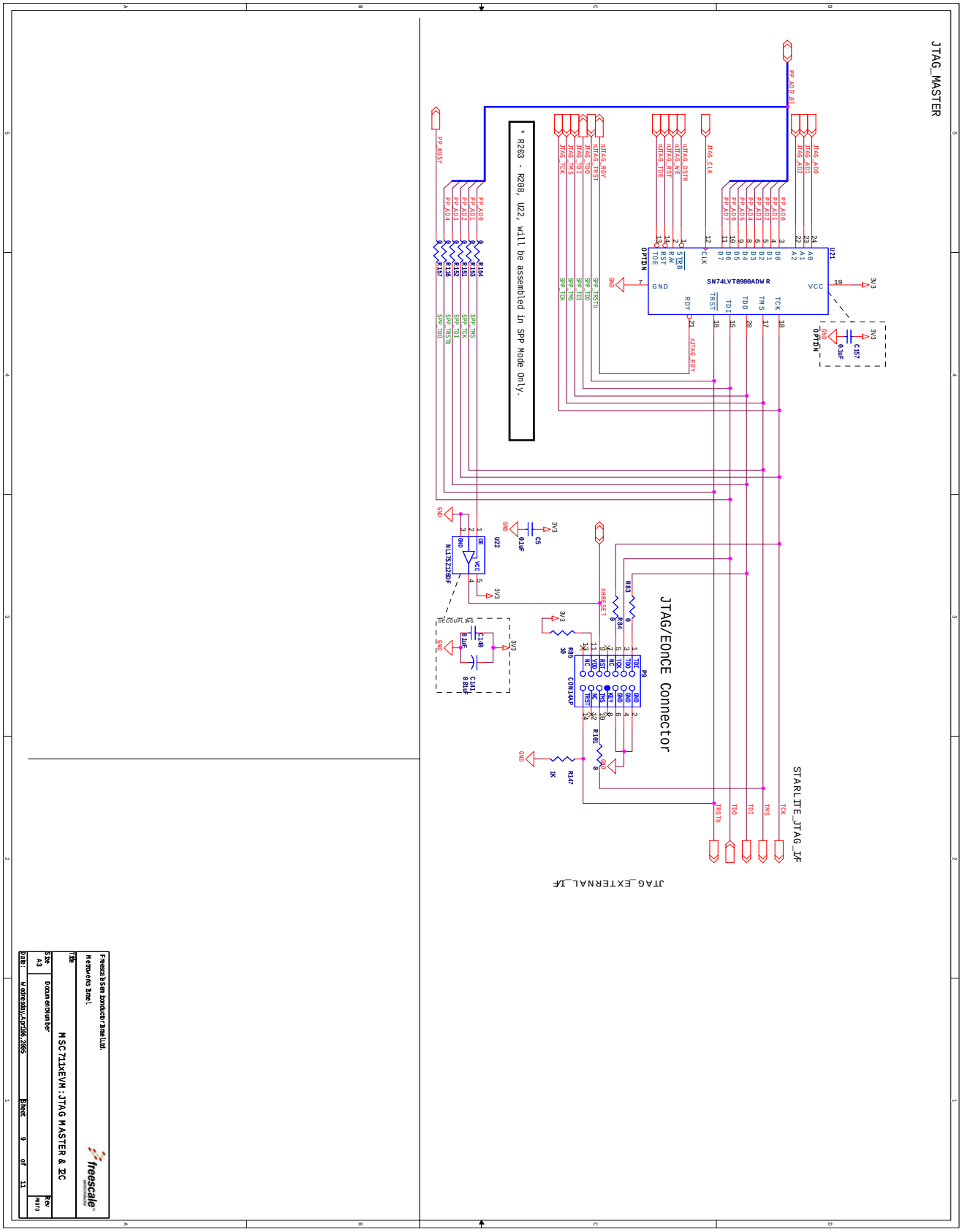
A.1.6 Ethernet



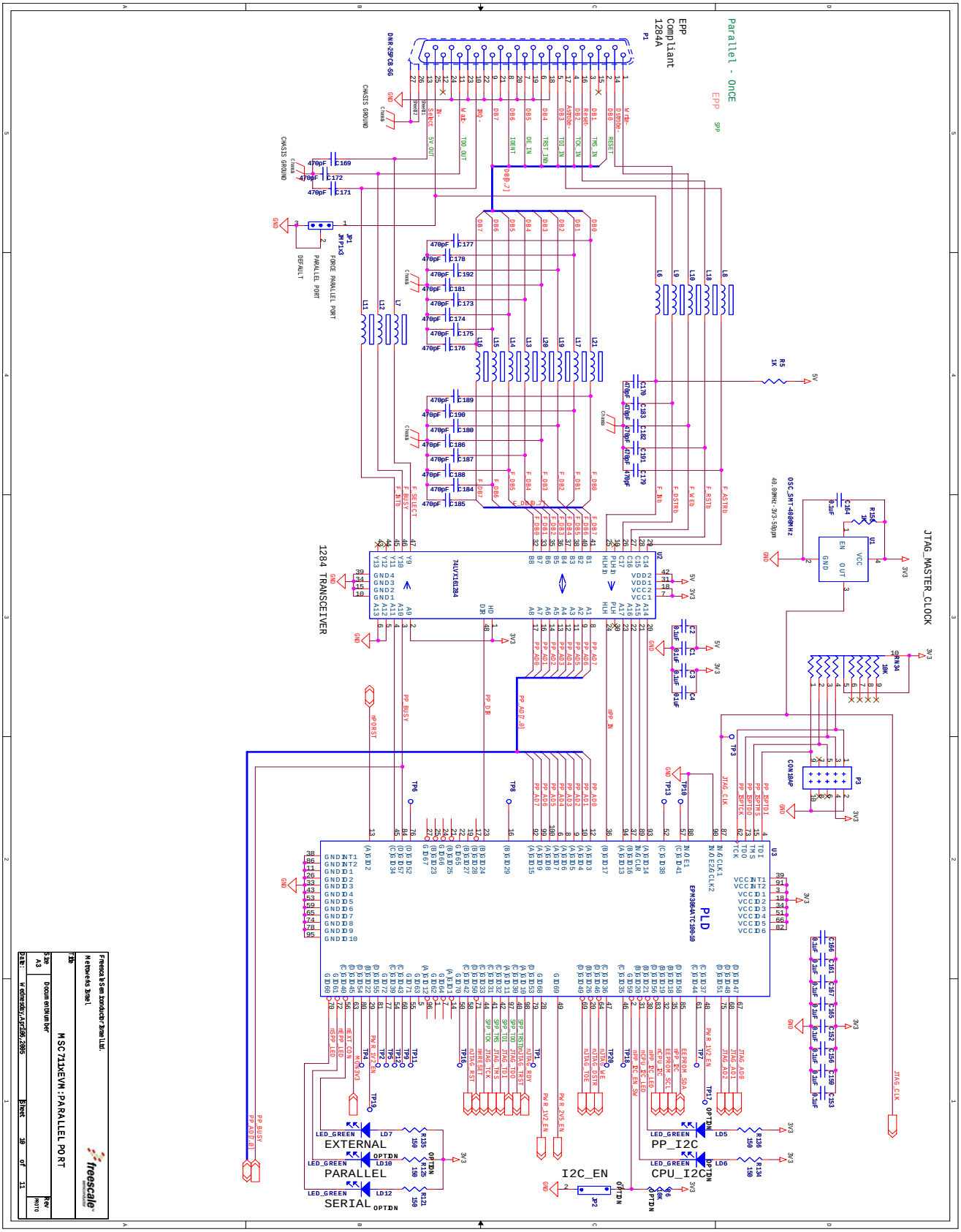
A.1.7 CODEC


P8
PHONO JACK STEREO 15_0
P7
PHONO JACK STEREO 15_0
U19
AKM AK4550
AINL
AINR
VCOM
AOUTL
AOUTR
VSS
VDD
MCLK
LRCK
SCLK
STDO
STDI
PWAD
PWDA
DEM0
DEM1
EVENT1
TDM0_RFS
TDM0_RCLK
TDM0_RD
TDM0_TD
nPORST
BEAD FERRITE
AGND1
GND
3V3
3V3A
5V
5VA
Freescale Semiconductor Israel Ltd.
Metrowerks Israel
MSC711xEVM:CODEC
Wednesday, April 06, 2005
Sheet 8 of 11

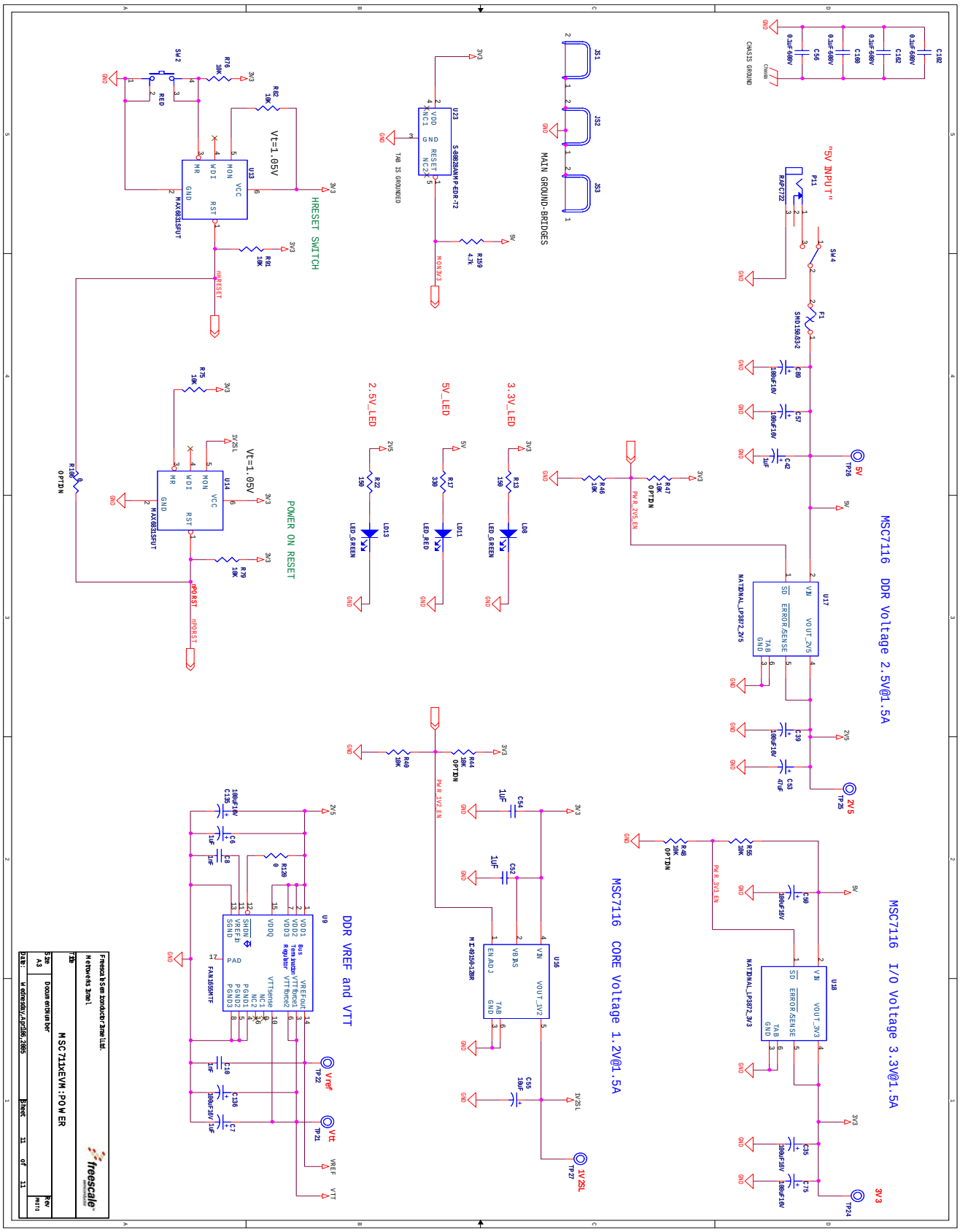
A.1.8 JTAG_Master



A.1.9 Parallel Port



A.1.10 Power


MSC7116 DDR Voltage 2.5V@1.5A
MSC7116 I/O Voltage 3.3V@1.5A
MSC7116 CORE Voltage 1.2V@1.5A
DDR VREF and VTT
POWER ON RESET
HRESET SWITCH
MAIN GROUND-BRIDGES
"5V INPUT"
2.5V_LED
5V_LED
3.3V_LED
MSC711xEVM:POWER